EDN®

THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

JUNE 22, 1995

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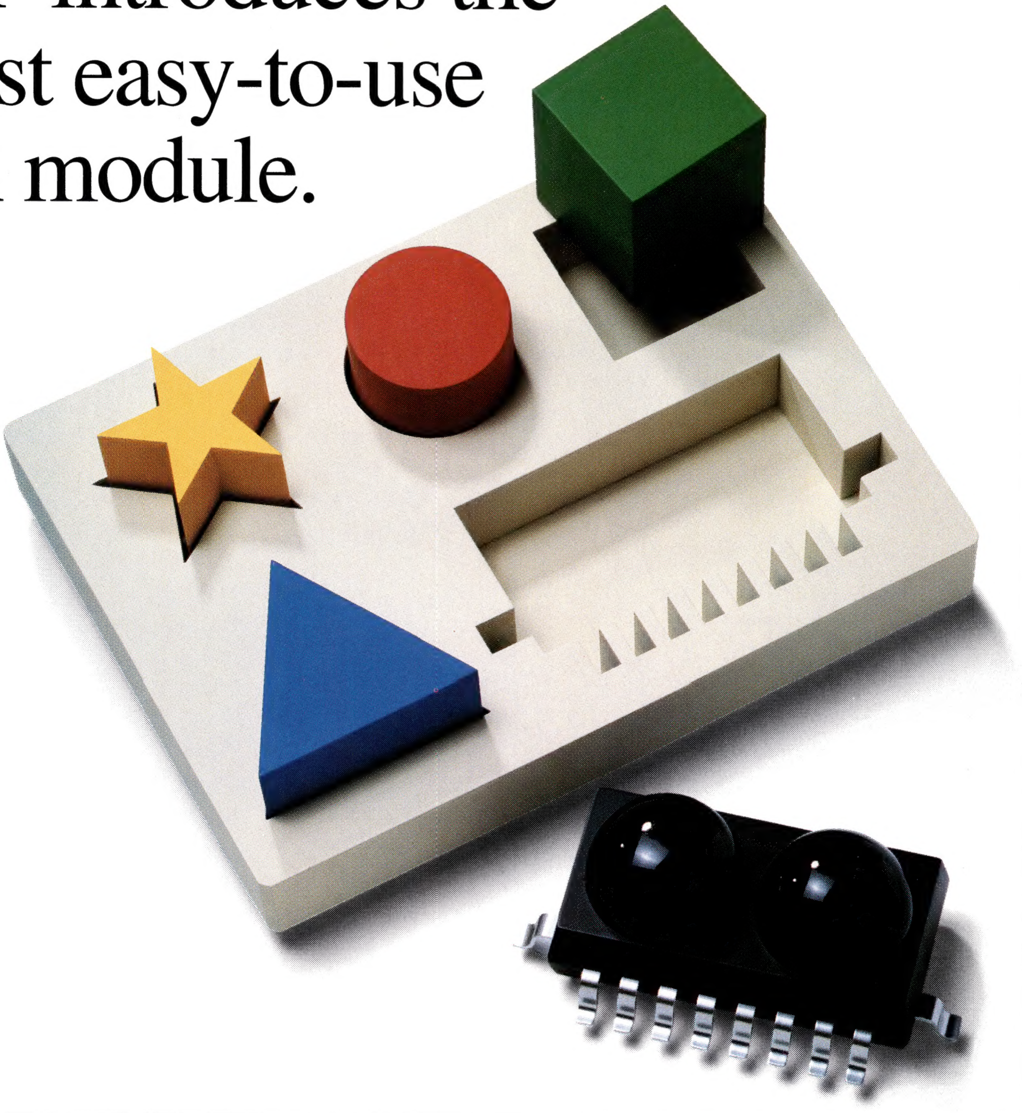

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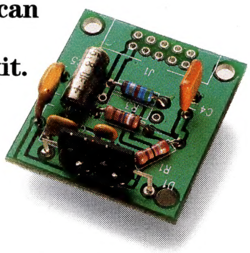

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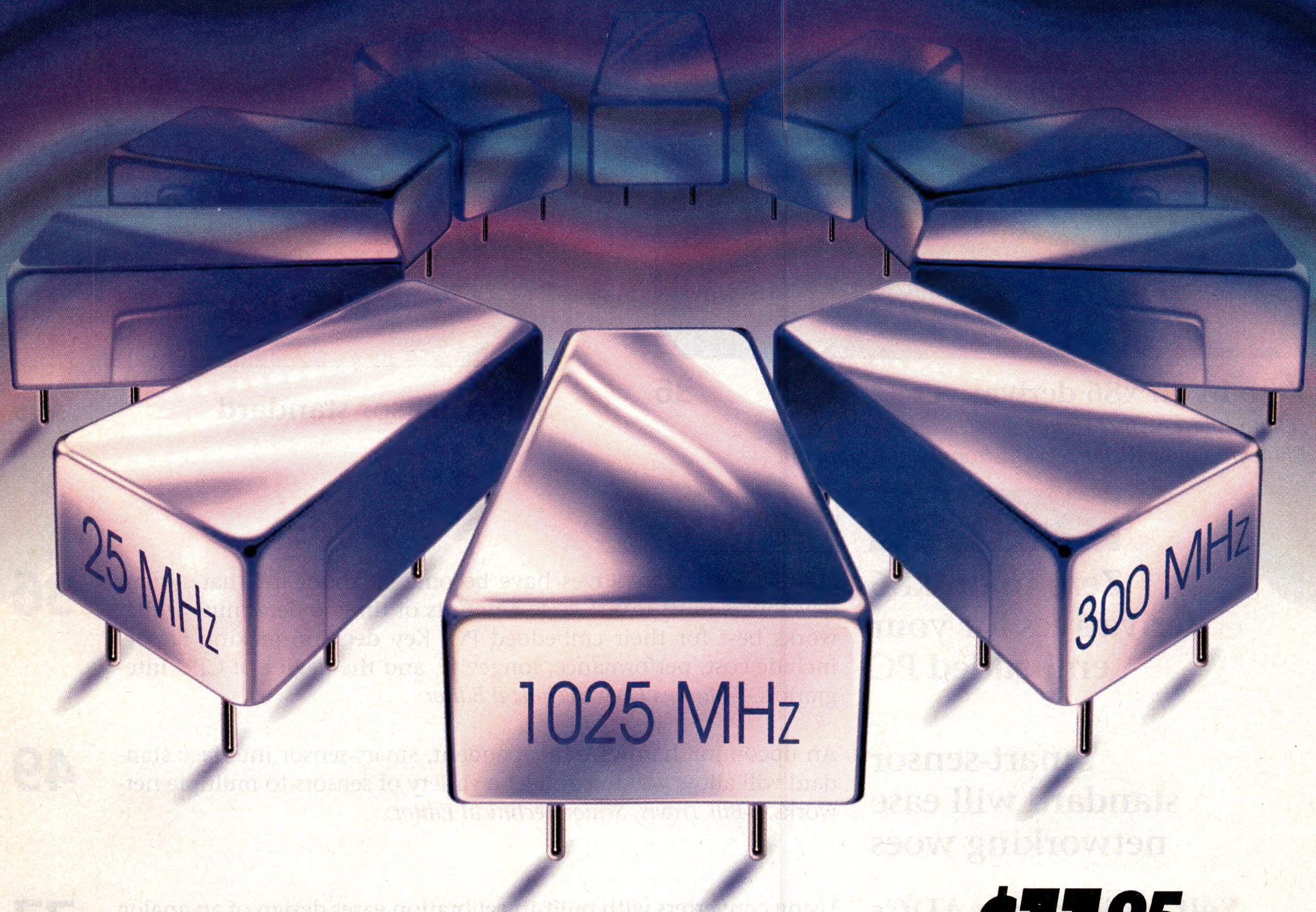

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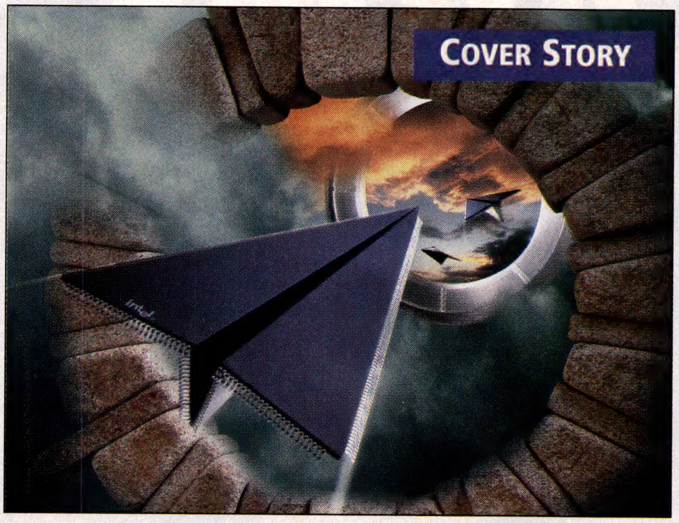
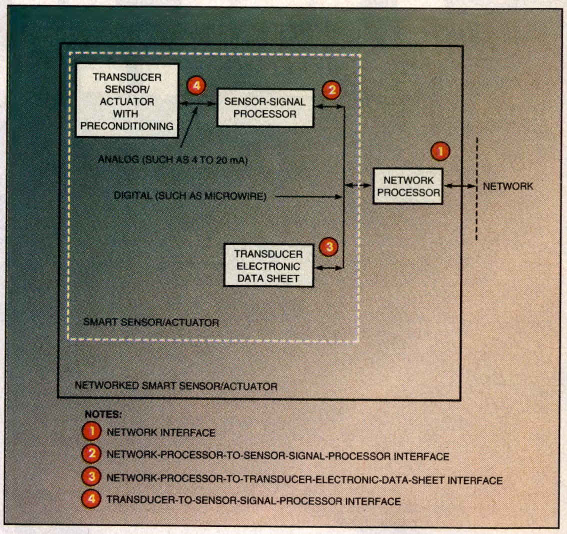


Zero in on x86 derivatives 36
(Photo courtesy Intel Corp)
Photography by Richard Wahlstrom Photography Inc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3 NETWORK-PROCESSOR-TO-TRANSDUCER-ELECTRONIC-DATA-SHEET INTERFACE
4 TRANSDUCER-TO-SENSOR-SIGNAL-PROCESSOR INTERFACE

Smart-sensor standard 49

EDN

DESIGN FEATURES

Zero in on x86 derivatives for your embedded PC

x86-processor derivatives have become so abundant that system developers must invest large amounts of time to determine which works best for their embedded PC. Key decision-making factors include cost, performance, longevity, and the degree of CPU integration.—*Markus Levy, Technical Editor* **36**

Smart-sensor standard will ease networking woes

An upcoming hardware-independent, smart-sensor interface standard will allow you to connect a variety of sensors to multiple networks.—*Bill Travis, Senior Technical Editor* **49**

Self-calibrating ADCs offer accuracy, flexibility

Using converters with built-in calibration eases design of an analog signal chain with greater accuracy and fewer calibration-related components. This calibration affects what you can achieve in accuracy and linearity and the hardware and software effort required.
—*Sean O'Leary, Analog Devices Inc* **77**

Parallel-printer adapters find new use as instrument interfaces

The venerable parallel-printer adapter has found many uses during its long lifetime. Now, you can use the port as an instrument interface—for connecting a photometer and a PC, for example.
—*Dhananjay V Gadre, Inter-University Centre for Astronomy & Astrophysics* **99**

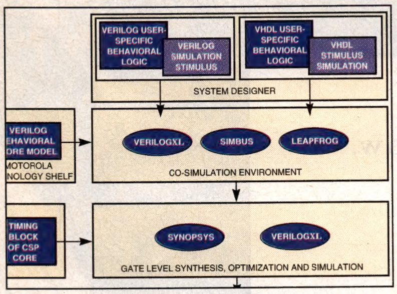
Manufacturing, design partnership reduces PC Card assembly costs

The traditional nuts-and-bolts approach to socket hold-down during reflow soldering gives way to an easier, faster method using metallic solder-retent pins.—*Bill Kuypers, Robinson Nugent Inc* **111**

Careful system analysis yields optimum IC-based PCMCIA power control

In designing power-management circuitry into a PCMCIA-standard PC Card, you face an economic trade-off between power-switch on-resistance and power-supply accuracy.
—*Bob Wolbert, Micrel Semiconductor* **121**

OUT IN FRONT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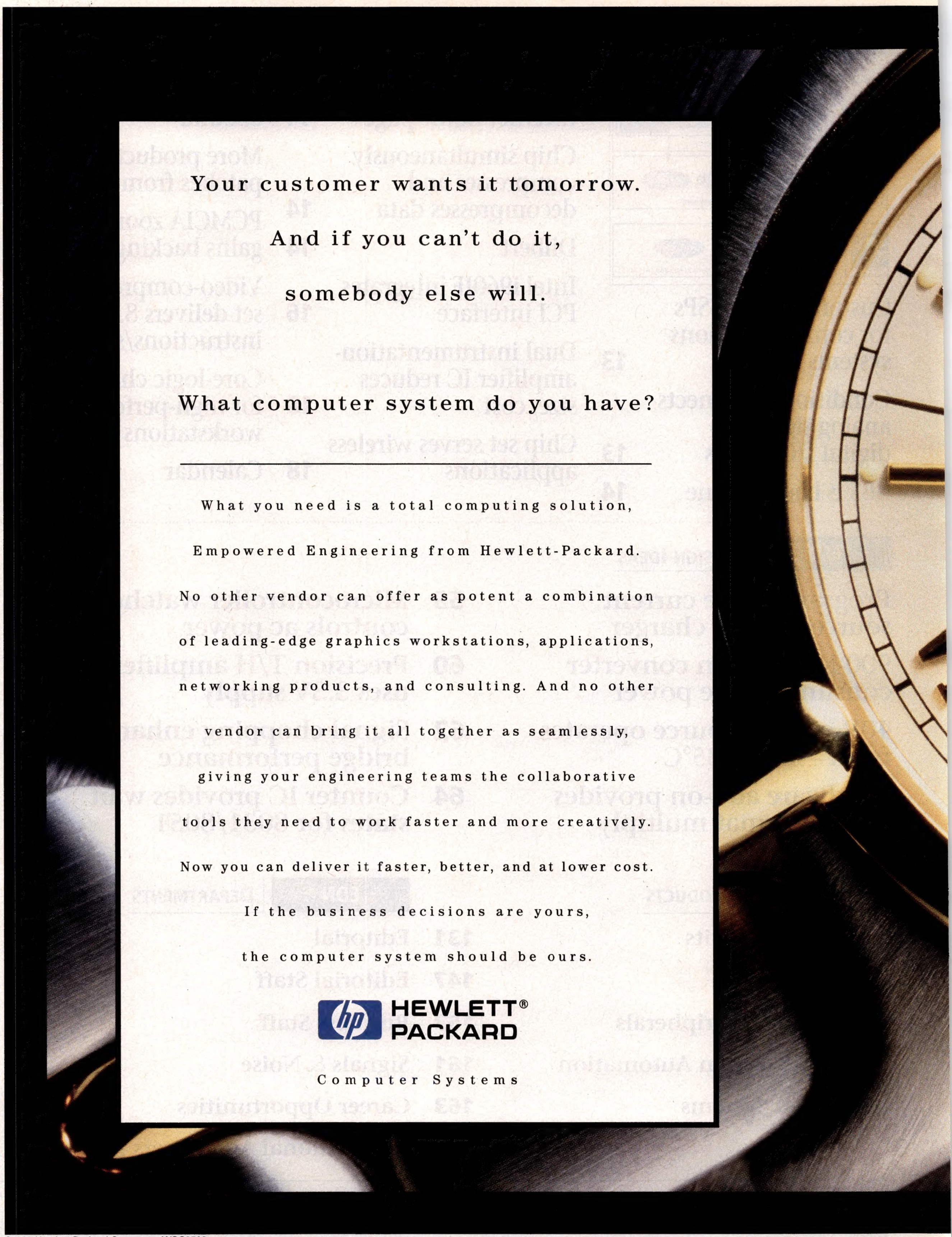

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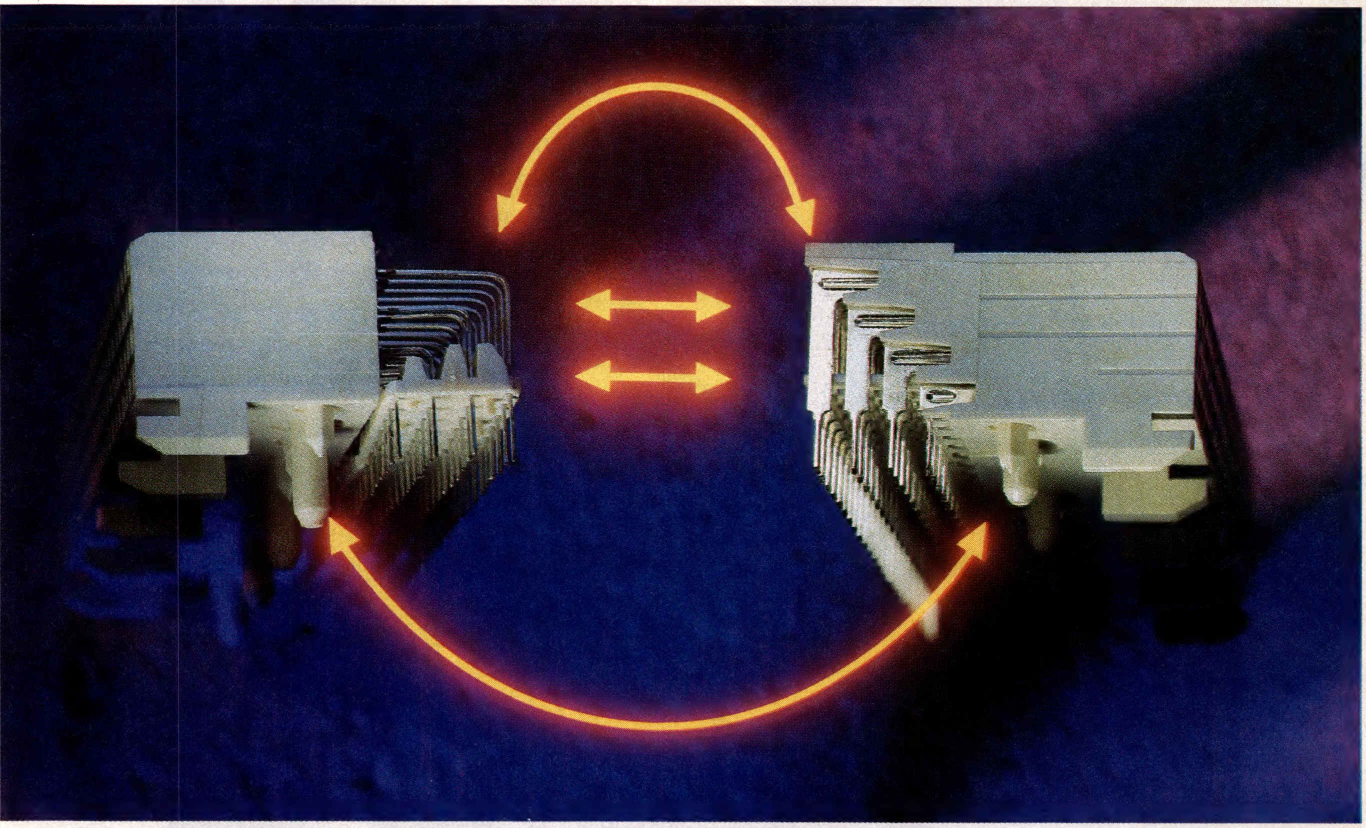

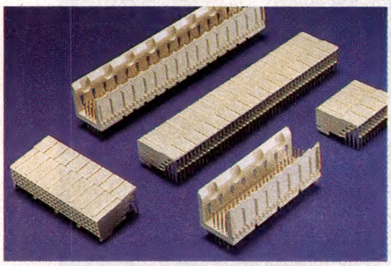

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RISC vs CISC: a dead horse

It's long been my position that the argument over RISC vs CISC is no more than a religious one. What we've witnessed over the past several years is simply a fight among competing µP architectures. I was reminded of this view recently during a presentation by John Bourgoin, group VP of microprocessor products at AMD, during In-Stat's 11th Annual Microelectronics Forum in Phoenix. Bourgoin's focus was on developing superscalar µPs that execute the x86 instruction set. He specifically focused on AMD's K5 processor. I think you, too, will find Bourgoin's points very useful the next time you find yourself in a "religious debate" over processor architectures.

> **In reality, x86-processor designers have found superscalar-RISC developments a treasure trove of ideas for improving their designs.**

First, Bourgoin reviewed the conventional wisdom surrounding the RISC-vs-CISC argument. The major claim made by RISC advocates is that architectures running the x86 instruction set will eventually run out of gas. This argument has several minor points. The first is that RISC instructions are "hard-wired" and are, therefore, inherently faster than CISC instructions. The second point is that the x86 architecture has serious general-purpose register limitations that force excessive memory accesses, thus slowing program execution. Next, some processor designers believe that the x86's variable-length instructions are difficult or impossible to decode in parallel, making it impossible to create a superscalar x86. Earlier x86s also had clumsy and slow memory accesses. All of these factors make it extremely difficult to create a wide-issue version of an x86 processor, and the simplicity of RISC instructions makes it easy to develop superscalar RISC µPs.

CISC-processor designers have ignored the impossibilities; there are now at least three superscalar x86 processors: AMD's K5, Intel's P6, and NexGen's 586. AMD's K5, for example, can issue four instructions at a time. The K5 does this by fetching x86 instructions from memory and predecoding them into fixed-length instructions, called ROPs (pronounced "ar-ops"), executed by multiple execution units. On average, 16-bit x86 instructions convert into 1.9 ROPs, and 32-bit x86 instructions translate into 1.3 ROPs. The K5 also makes use of reorder buffers to allow out-of-order execution, just as RISC processors do.

Advances in IC fabrication make millions of transistors available to all processor designers. RISC-processor designers use these extra transistors for floating-point units and bigger caches. CISC designers use the extra transistors to systematically reduce the number of cycles required to execute each instruction. It all boils down to the ability to execute more than one instruction per cycle, no matter which side of the argument you're on. And, in the end, the right architecture is the one that gets the job done for you.

Steven H. Leibson

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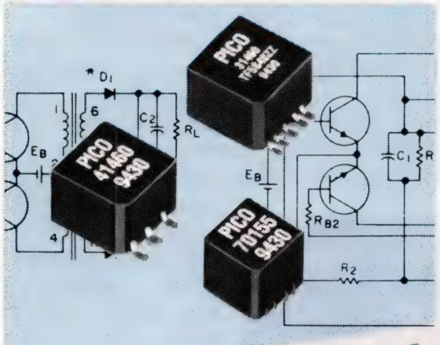

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CIRCLE NO. 91

Noritake

Introduces the New 2 x 20 U-Version Module

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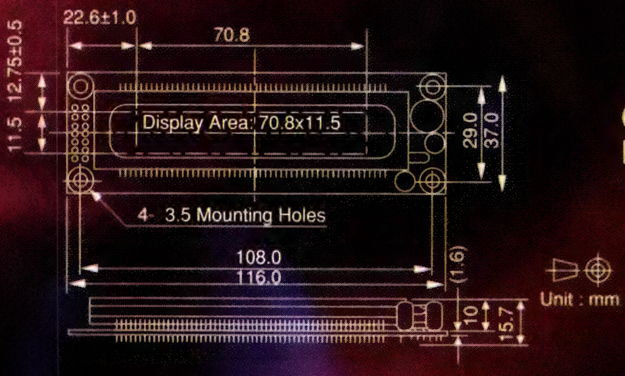

Compatibility with LCD Module with LED backlight:

- Function of the Controller Chip
- Locations of interface through holes and mounting holes
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CIRCLE NO. 92

EDN OUT IN FRONT

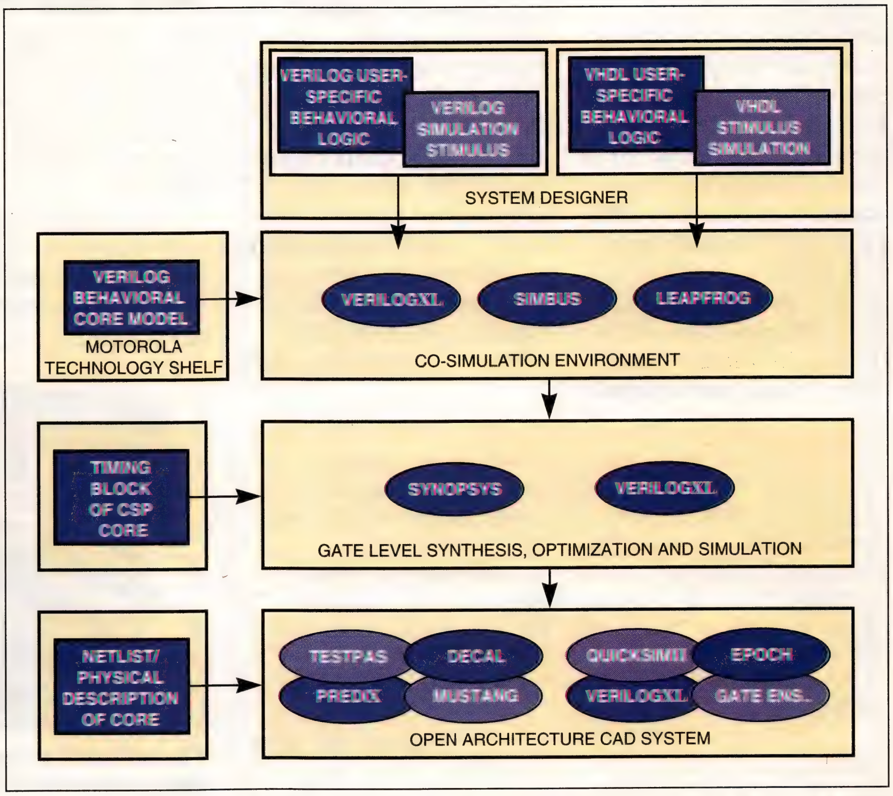
EDITED BY FRAN GRANVILLE

Customizable ASSPs for communications systems

Motorola has announced the Customized Standard Products (CSP) program to allow you to develop and customize application-specific standard-product (ASSP) chips. The program allows you to combine highly integrated, predefined complex functional blocks (CFBs) with user-defined logic and memory. With CSP, you can tailor your chip design to an application in a gate-array or cell-based implementation.

CSP is similar to VLSI Technology's functional-system-block (FSB) approach to ASIC-chip design. FSB cells are also application-specific, predefined blocks of complex logic that you can embed into a chip and then surround with random logic and peripheral blocks. Motorola's initial offerings, however, aim directly at the networking and communications markets and would benefit from the company's experience in this arena.

The first CSP chips target communication systems and include an asynchronous-transfer-mode (ATM) cell processor implementing ATM-layer functions for broadband integrated-services digital-networks applications. Motorola plans to add customizable products for ATM segmentation and reassembly (SAR), digital TV, and high-speed-interface standards, such as fibre channel.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SIMBUS
LEAPFROG
CO-SIMULATION ENVIRONMENT
TIMING BLOCK OF CSP CORE
SYNOPSYS
VERILOGXL
GATE LEVEL SYNTHESIS, OPTIMIZATION AND SIMULATION
NETLIST/ PHYSICAL DESCRIPTION OF CORE
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DECAL
QUICKSIMII
EPOCH
PREDIX
MUSTANG
VERILOGXL
GATE ENS.
OPEN ARCHITECTURE CAD SYSTEM

Motorola's CSP design flow uses third-party tools and is compatible with both VHDL and Verilog.

The communication-specific CFBs will also operate in a family of ASSPs, part of Motorola's MC92000 series. The first members of this family include the MC92516, a 155-Mbps ATM SAR controller with Utopia interface or synchronous-optical-network framer, and the MC92500, an ATM cell processor with Utopia interface ports.

CSP-program NRE fees start at approximately $100,000. Actual NRE charges vary with the complexity of customization and include the cost of integrating user-specific logic with Motorola's predefined cores, final chip layout, and delivery of tested prototype chips.—by Jim Lipman

Motorola Inc, Phoenix, AZ. (602) 952-3856. **Circle No. 435**

Conditioner connects analog signals to digital I/O points

What happens when you need to monitor or provide an analog signal but no unused analog inputs or D/A outputs remain on your programmable logic controller (PLC) or PC-based data-acquisition board? The new SensorPulse 2000 signal conditioner from Interactive Process Controls can come to the rescue. The µP-based 4.5×3.825-in. DIN-rail-mountable devices convert analog inputs to a one-wire form for driving PLC- and I/O-board digital inputs. The units can also convert trains of pulses from PLC- or I/O-board digital outputs to analog voltages or currents.

Because you must provide conditioning for most sensor signals you would normally connect to PLC or I/O-board analog inputs, SensorPulse often involves no additional hardware or expense. The units accept signals from a variety of sources, including current loops and frequency sources, such as rotation-speed sensors; thermocouples, for which SensorPulse provides cold-junction compensation and linearization; and bridges, resistance-temperature detectors (RTDs), and potentiometers, for which SensorPulse provides excitation.

One drawback of the SensorPulse approach, albeit for only a few industrial users, is frequency response. When

(continued on pg 14)

you connect a SensorPulse output to a PLC digital input, the speed of response depends on how much the PLC filters the SensorPulse's output pulse train. Some PLCs' filters limit the data rate to 10 or fewer readings/sec. Data-acquisition boards, on the other hand, usually provide little or no filtering, so they permit hundreds of readings/second (with the two-channel SensorPulse, which uses a delta-sigma ADC; the single-channel unit uses a multiple-slope ADC, which makes up to 60 readings/sec). The SensorPulse units operate from a 20 to 30V-dc power supply. A single-channel unit costs $200, and a two-channel unit costs $300.

—by Dan Strassberg

Interactive Process Controls Corp, South Easton, MA. (508) 230-9000. **Circle No. 436**

Distributor puts up Internet home page. Hamilton Hallmark's home page provides on-line Hypertext links to the company's suppliers' Internet pages, application support, reference designs, technical articles, data sheets, and lead-time and pricing trends by product commodity. The home-page address is: ttp: WWW.TSC.HH.AVNET.com on the World Wide Web. **Hamilton Hallmark**, Division of Avnet Inc, Culver City, CA. (800) 605-3294.

Circle No. 437

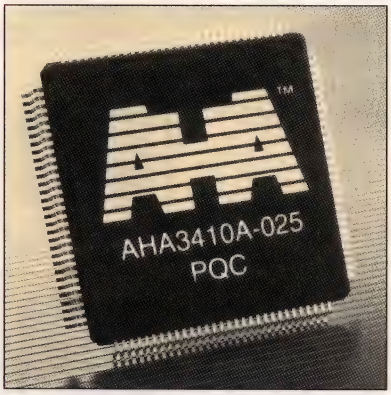
BBS is back on-line

EDN's computer bulletin-board system (BBS) is now back on-line after having experienced some technical difficulties. We apologize for any inconvenience you may have experienced. To access the BBS, phone (617) 558-4241 with modem settings 300/1200/2400 8,N,1.

CHIP SIMULTANEOUSLY COMPRESSES AND DECOMPRESSES DATA

The single-chip AHA3410 from Advanced Hardware Architecture can simultaneously execute lossless compression and decompression for bitonal images. The chip allows high-resolution printers and copiers to print a page while compressing another page in the background.

The chip compresses and decompresses data at 25 Mbytes/sec and handles a 100-Mbyte/sec burst data rate over a 32-bit bus. The speed enables the chip to process over 90 pages/minute at 1200 dpi on standard 8.5×11-in. documents. Typical compression ratio for bit-mapped image data is 4-to-1; however, the device can achieve higher ratios, depending on image-data complexity.



The AHA3410 compresses and decompresses data at 25 Mbytes/sec.

The chip incorporates scanner input and printer output for multifunction devices, such as network printers, copiers, and scanners. It also provides a glueless interface to Advanced Micro Devices' 28K, Intel's 960, and Motorola's 68K embedded processors in most printers and copiers. The chip's lossless compression algorithm suits high-resolution single-bit/pixel printer and copier applications. Production will begin in the fourth quarter; price is approximately $30. Samples are available now.

—by John Gallant

Advanced Hardware Architecture Inc, Pulham, WA. (509) 334-1000. **Circle No. 438**

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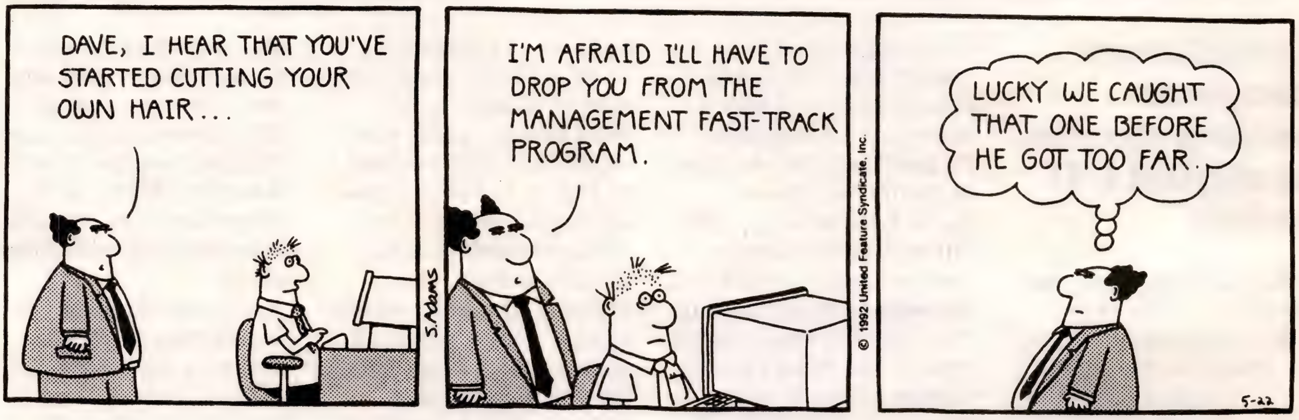
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S.Adams
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LUCKY WE CAUGHT THAT ONE BEFORE HE GOT TOO FAR.
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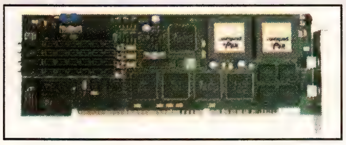

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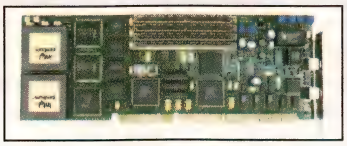

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CIRCLE NO. 160

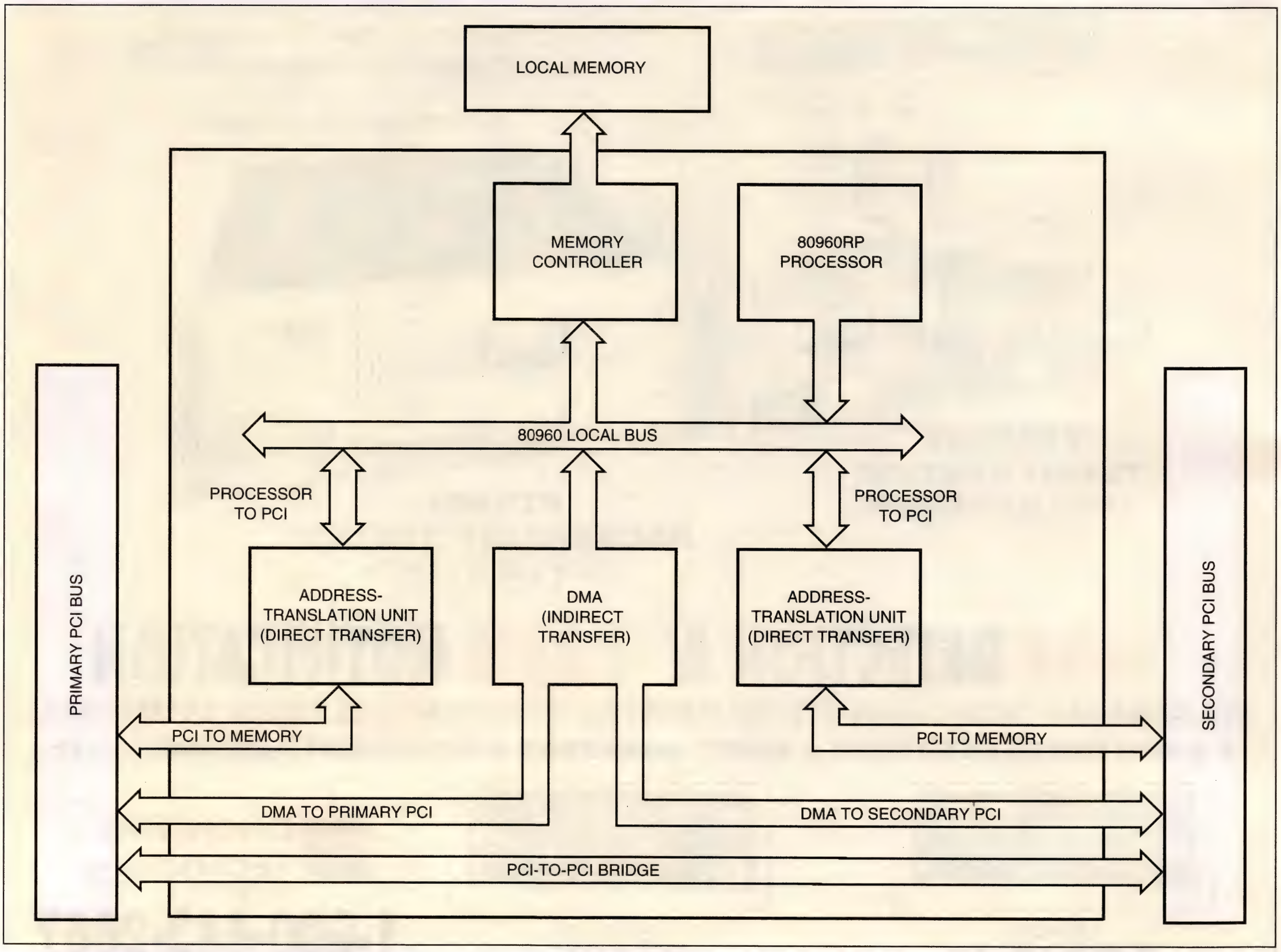
Intel i960JF integrates PCI interface

As the Peripheral Component Interconnect (PCI) bus grows in popularity, Intel and others (as yet unannounced) are following in the footsteps of Digital Equipment, the first to integrate a PCI bus interface directly onto a µP, the Alpha 21066. This interface allows the 21066 to attach directly to the PCI bus and to function as both a master and a target PCI device.

Intel adds its i960JF to PCI-to-PCI-bridge circuitry to create one chip, called the i960RP, "a single-chip, intelligent-I/O subsystem." The device targets I/O-intensive applications such as asynchronous transfer mode, redundant array of individual disks (RAID), and multiport Ethernet. Although you can use a PCI-to-PCI bridge chip to connect a PCI-based I/O subsystem to any host system's primary PCI bus, these bridge chips are relatively unintelligent. However, adding a processor to this bridge allows that processor to handle incoming and outgoing data, instead of immediately passing it to the host CPU. This approach reduces interrupts to the host CPU and, therefore, enhances overall system performance.

The PCI interface on the i960RP bridges the primary and secondary PCI buses. This approach allows the primary bus to be the system bus of the host platform and the secondary bus to connect as many as 10 PCI peripheral devices, assuming each device represents only one load. To avoid the need for an external arbiter, the i960RP includes a PCI bus arbiter and associated request/grant pins, which support up to six masters on the secondary PCI bus. The i960RP also has an internal local-bus-arbiter unit (LBAU) that controls the bus mastership of the i960's local bus. The LBAU allows the i960RP's two integrated DMA units to take ownership of the local bus while the i960RP passes data or code between the primary or secondary side of the bridge and the i960RP's local memory. While moving the data, the DMA units use on-chip, 64-byte FIFO buffers to reduce latency and increase throughput. The

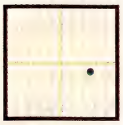
(continued on pg 18)



The i960RP bridges data transfers between the primary and secondary PCI buses and performs direct and indirect data transfers between the primary or secondary PCI buses and the local bus.

Get a sample of reality.

Looking for analog confidence in a digital oscilloscope? Tektronix' TDS 350 sets the standard with Digital Real Time. ▪ Its incredible *one gigasample / second* sampling delivers real-life capture like never before — both for single shot or repetitive events. Select peak detect for slow events, or push the scope to its full 200 MHz bandwidth — while minimizing aliasing. ▪ And, like the entire TDS 300 family, the TDS 350 sets a new standard in price/performance.



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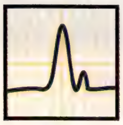

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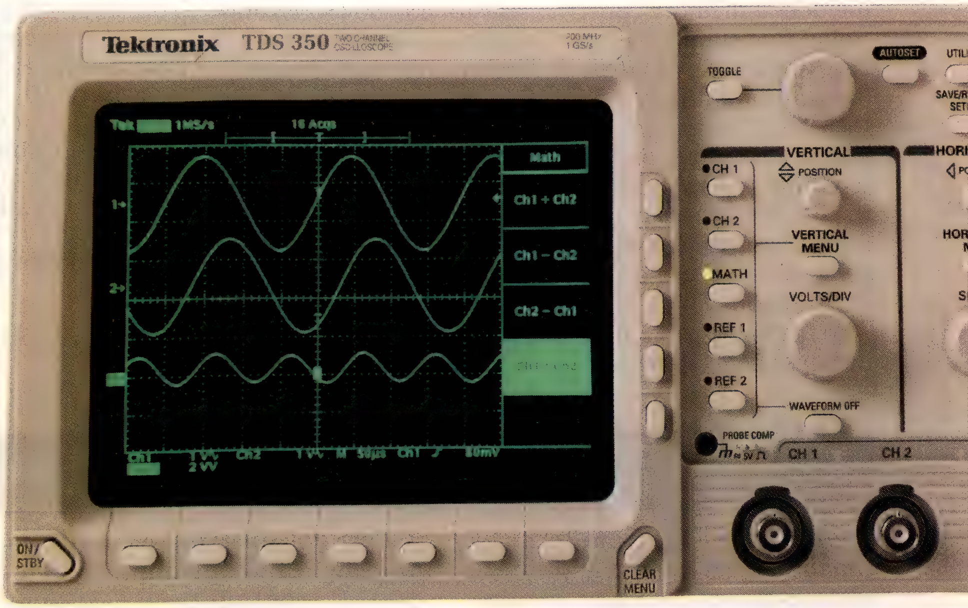

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Vertical Resolution	8 bits	8 bits	8 bits
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Tektronix

PCI-to-PCI bridge also contains dual 64-byte buffers to support both downstream (primary-to-secondary) and upstream (secondary-to-primary) transactions.

The i960RP also includes a memory controller that supports up to 256 Mbytes of extended-data-out or fast-page DRAMs, an interrupt controller, and an I²C interface. In RAID applications, the I²C interface can transfer power- and temperature-monitoring information.

Many third-party and in-house development tools, including real-time kernels, C compilers, and emulators, support the i960RP. Intel is also working with several software vendors to provide drivers for the i960RP's targeted applications. The i960RP sells for $57.50 (1000) and will be available in the first quarter of next year.

—by Markus Levy

Digital Equipment Corp, Maynard, MA. (508) 568-6868.
Circle No. 439

Intel Literature Center, Mount Prospect, IL. (800) 468-8118.
Circle No. 440

DUAL INSTRUMENTATION-AMPLIFIER IC REDUCES SIZE, COST

For multichannel data-acquisition systems, Burr-Brown's INA2128 puts two instrumentation amplifiers into a single 16-pin package (DIP and SOIC). Each channel provides a three-op-amp configuration with on-chip, laser-trimmed resistors and consumes 600 µA. An external resistor sets gain from 1 to 10,000; bandwidth is 200 kHz at a gain of 100 and 700 kHz at a gain of 10. The device can withstand inputs up to ±40V with or without power applied. The device features a maximum offset voltage of 50 µV, an offset voltage drift of 0.5 µV/°C, and an input-bias current of 5 nA. It operates from a ±2.25 to ±18V supply and costs $5.60 (1000).—by Bill Schweber

Burr-Brown Corp, Tucson, AZ. (800) 548-6132.
Circle No. 441

CHIP SET SERVES WIRELESS APPLICATIONS

A family of RF ICs from Telefunken comes in small-outline, surface-mount packages, easing wireless design for Advanced Mobile Phone Service, Global System for Mobile, and wireless-LAN applications. The chip set includes three ICs for the transmit path, two for the receive path, and a PLL frequency synthesizer.

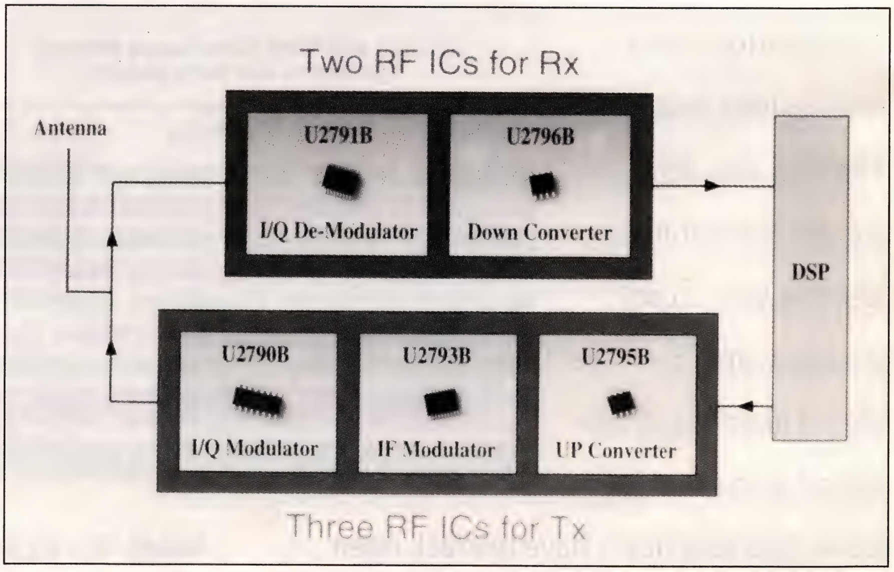
On the transmit side, the U2795B double-balanced mixer operates as an up-converter or a down-converter from 50 MHz to 2.5 GHz and is useful in dual-conversion applications. Another IC, the U2793B, functions as a quadrature IF modulator for operation from 30 to 300 MHz. Sideband suppression is 45 dB at 150 MHz. The U2790B, a direct-conversion quadrature modulator, operates at 100 to 1000 MHz; output power is −1 dBm, and power consumption is 150 mW.

For the receive channel, the 1000-MHz U2791B quadrature demodulator works with the U2796B, a 2-GHz down-conversion mixer, which has gain and noise figures of 9 dB each. For either transmit or receive, the U2781 PLL operates to 1.1 GHz; a three-wire bus operating at up to 500 kHz controls the U2781's programmable prescaler and other functions.

All devices operate from a nominal 5V supply, and some can also use a 3V supply. Current consumption ranges from 5 to 28 mA, depending on device; where appropriate, the ICs include a power-down mode. Prices range from $2.25 to $5.75 (10,000).

—by Bill Schweber

Telefunken Semiconductors (Temic), Santa Clara, CA. (800) 554-5565, ext 57. **Circle No. 442**



A family of RF devices from Telefunken for wireless-phone and -LAN applications includes three ICs for the transmit path, two for the receive path, and a PLL synthesizer.

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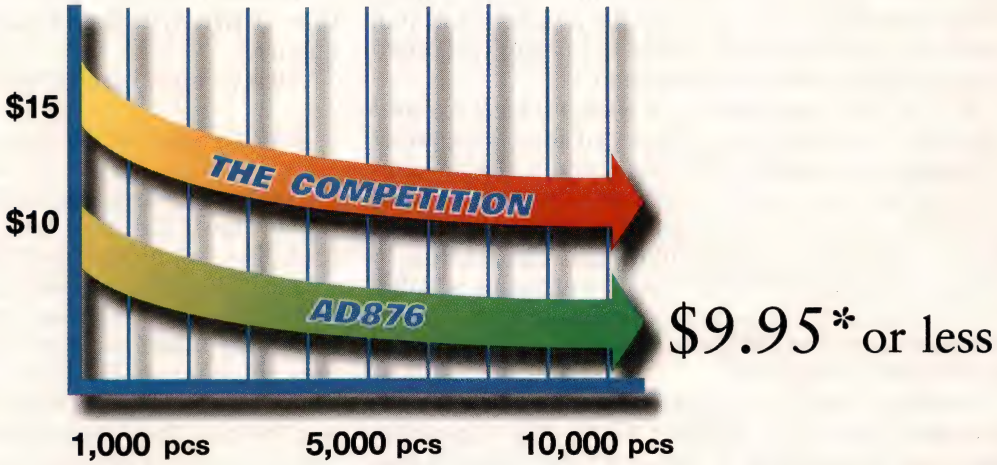

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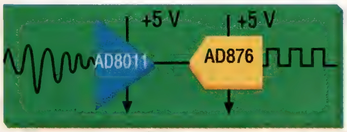

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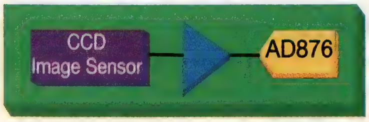
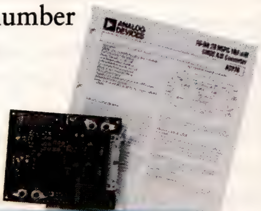


Why Overpay? For samples, evaluation board or technical information, call the number listed below, or fax your request to 617-821-4273. For data sheets only, dial the number listed below and enter faxcode #1838 when requested. For a data sheet on our 1 mA, 300 MHz AD8011 op amp use Faxcode #1863.



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NEW EDA ALLIANCES ABOUND

The past few months have seen a plethora of partnering agreements among vendors to bring customers faster and better design tools and systems. Many of these efforts aim at broadening either the capabilities of tool suites or increasing their ability to operate with standardized data formats or other tools.

In one such agreement, Hewlett-Packard Co and Viewlogic Systems have announced joint support of interfaces that integrate HP EEsof's high-frequency simulation software with Viewlogic's Powerview and Workview design environments for Unix and PC platforms, respectively. The combination enables you to design a system, including RF baseband analog and digital circuits, on one electronic-design-automation (EDA) system using one database. This capability should speed system-design time.

Viewlogic has also strengthened its partnership with pc-board design-tool supplier PADS. The companies intend to integrate the design of IC and pc-board portions of a system into a common design environment and to create system-design standards for the electronics industry. The bond also gives Viewlogic a stronger position in the Vendor Integration Alliance (VIA) program, which PADS developed to combine its pc-board-design systems with third-party tools for analysis, mechanical CAD, test, and manufacturing.

HP EEsof, Westlake Village, CA. (818) 879-6200. **Circle No. 443**

PADS Software, Marlborough, MA. (508) 485-4300. **Circle No. 444**

Viewlogic Systems, Marlborough, MA. (508) 480-0881. **Circle No. 445**

Two Silicon Valley companies, CrossCheck Technology and Silicon Valley Research (SVR), plan to develop an interface to integrate SVR's GARDS place-and-route tool with ArrayTest, CrossCheck's embedded technology for gate-array test-pattern generation and debugging. The combination speeds physical layout and testing of gate-array designs. CrossCheck also claims that ArrayTest achieves 10 to 15% higher gate utilization than chips using traditional scan techniques for testability, making more efficient use of the silicon area.

CrossCheck Technology, San Jose, CA. (408) 432-9200. **Circle No. 446**

Silicon Valley Research, Mountain View, CA. (415) 962-3000. **Circle No. 447**

Acknowledging the rising role of DSP components in digital chips, Alta Group of Cadence Design Systems and DSP Group have simplified DSP-system design. Alta Group, a vendor of high-level EDA tools, has placed instruction-level models from DSP Group's core DSP technology into Alta's electronic-systems-design-automation products. The combination provides a common specification for designing, partitioning, and verifying DSP systems' hardware and software components. The combination also lets you determine early in the design whether the hardware and software are behaviorally compatible before silicon is available for testing. DSP Group's PineDSPCore and OakDSPCore models and interface products work with Alta's Hardware Design System and will be available in the third quarter.

Alta Group, Foster City, CA. (415) 574-5800. **Circle No. 448**

DSP Group, Santa Clara, CA. (408) 986-4300. **Circle No. 449**

Two other companies, Eonic Systems and VLSI Technology, have agreed to design real-time development tools. The first product will port Eonic's Virtuoso Nano to VLSI's PineDSPcore with technology licensed from DSP Group. Virtuoso Nano provides a multitasking programming model without the overhead of an operating-system kernel. The tool is especially useful in implementing the asynchronous data flows in DSP applications. Both companies will probably address DSP Group's Oak core with future efforts. Eonic also intends to port more of its software-development products to other VLSI DSP cores.

Eonic Systems, Silver Spring, MD. (301) 572-5000. **Circle No. 450**

VLSI Technology, San Jose, CA. (408) 434-3000. **Circle No. 451**

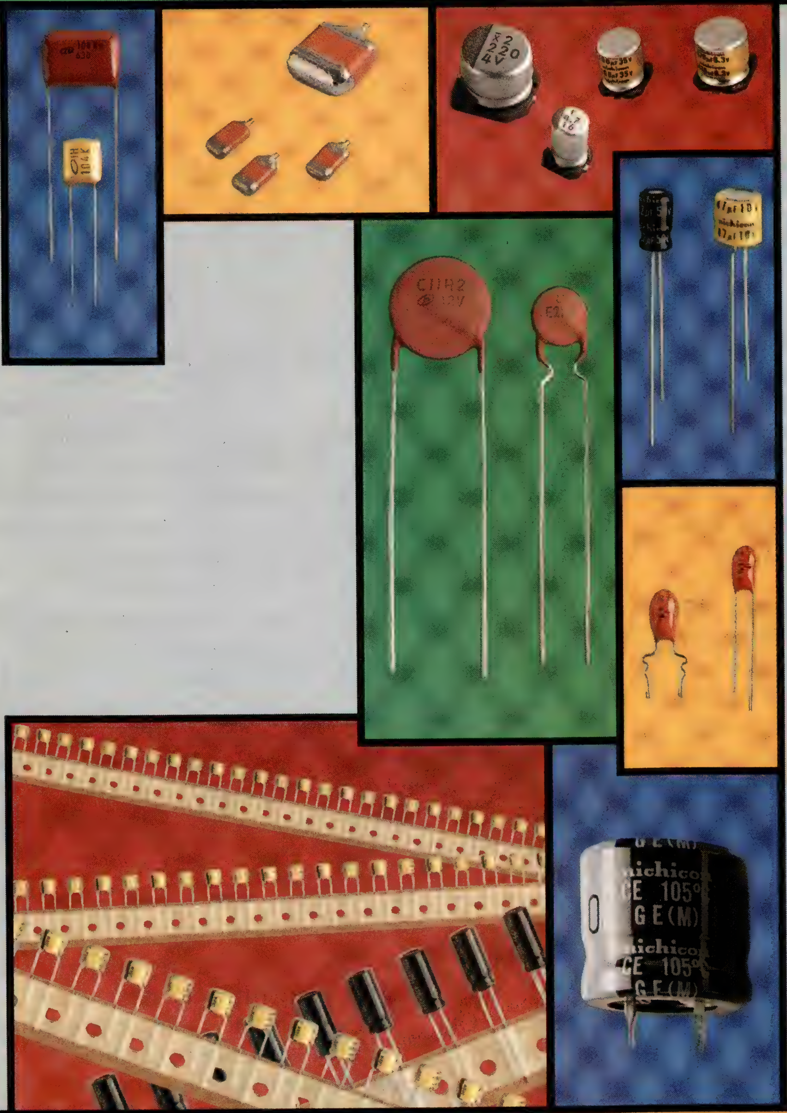
Escalade and Model Technology, a Mentor Graphics company, have signed an agreement to give Escalade the rights to provide Model Technology's V-System/VHDL simulator as part of Escalade's DesignBook tool suite. DesignBook lets you capture your design by a variety of graphical and hardware-description-language methods. You can then simulate the design with the V-System/VHDL tool, speeding debugging and verification. DesignBook also lets you enter constraint information and create code for a targeted synthesis tool. When released this year, DesignBook provided an interface to the V-System/VHDL simulator. The agreement between Escalade and Model Technology provides a more integrated system for high-level design automation.

Escalade, Sunnyvale, CA. (408) 481-1300. **Circle No. 452**

Model Technology, Beaverton, OR. (503) 641-1340. **Circle No. 453**

Although not strictly a partnering deal, Epic Design Technology's intent to buy Archer Systems, a developer of RC-extraction tools, is worth noting. Epic's new RailMill product, which helps you find electromigration and voltage-drop problems in a chip design before it goes to silicon, uses a modified version of Archer's Arcadia. Epic plans to sell Arcadia as a stand-alone layout-extraction tool and to use it in other tools to provide enhanced extraction capability.—by Jim Lipman

Epic Design Technology, Santa Clara, CA. (408) 988-2997. **Circle No. 454**



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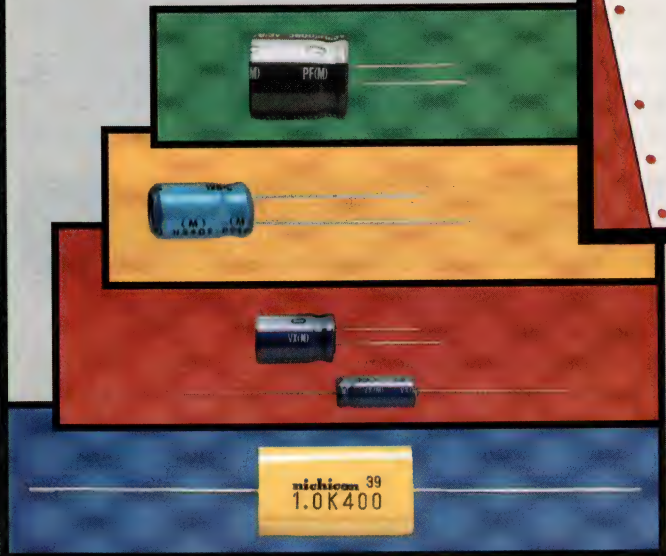

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CIRCLE NO. 94

More product dispatches from DSPx

Among the product introductions from last month's DSPx signal-processing conference and exhibition are the MathWorks DSP block set for its Signal Processing Toolbox and Simulink development package, which is based on the company's Matlab computing environment. Simulink lets you quickly explore alternative algorithms by assembling system block diagrams from predefined and custom building blocks. Once you refine your algorithm or system, Simulink generates C source code for incorporation into hardware. The $395 DSP block set runs on PCs and Macintosh computers and adds common DSP functions to Simulink. Matlab, Simulink, and the Signal Processing Toolbox cost $1695, $1995, and $395, respectively.

The MathWorks Inc, Cambridge, MA. (508) 653-1415.

Circle No. 455

DSP Software Engineering introduced VoiceWave, a proprietary, multirate, speech-compression algorithm that provides a 4-kHz channel bandwidth using 4.8- to 13.2-kbps digital bit streams. The company claims that this scheme maintains high speech quality at lower bit rates than do other schemes. The algorithm requires relatively little processor bandwidth; the decoder requires only 2 MIPS. Two full-duplex voice channels can run on a 60-MHz TMS320C32 DSP µP using less than 8 kbytes of external memory. The company negotiates software licenses for this technology individually.

DSP Software Engineering Inc, Bedford, MA. (617) 275-3733.

Circle No. 456

Pentek introduced two VME cards for embedded systems: the Model 6472, a dual 70-MHz A/D converter board, and the Model 4273, a time-code-reader/generator card. The $7995 high-speed A/D converter is especially useful for implementing digital receivers. Digital receivers can discriminate narrow bandwidths at high frequencies. For example, you can look at a 1-MHz slice in the 20- to 21-MHz region. The $2495 time-code-reader/generator employs daughtercards that can decode IRIG B, 2137, XR3, and NASA 36 time codes.

—by Steven H Leibson

Pentek Inc, Norwood, NJ. (201) 767-7100.

Circle No. 457

PCMCIA zoom video gains backing

Support is growing for a proposed zoom-video (ZV) PCMCIA standard that will allow a 27-Mbyte/sec video connection from a PC Card to a computer's display controller. Notebook computers that implement the standard will likely debut at Comdex in November, giving notebook users a foundation for desktoplike video applications, including video playback and conferencing.

The ZV connection bypasses the regular PCMCIA bus and sends video data directly to a computer's video frame buffer. The PCMCIA bus remains available for simultaneous transfers of other types of data (with some limitations) between the computer and a plugged-in PC Card. In theory, a ZV-capable PC Card in a ZV-capable computer can contain both a video application, such as a Moving Picture Experts Group (MPEG) decoder, and another function, such as a fax/modem.

ZV mode redefines 21 pins of the PCMCIA interface, including 18 of 26 address bits. Digital YUV video uses 19 of the redefined pins, and digital audio uses the other two. Of the 19 video pins, 16 carry video data, and the other three provide horizontal and vertical sync and a pixel clock. ZV mode does not use a PC Card's normal control, status, or data bits, but it does use 4 address bits and reserves use of 4 more bits. Consequently, simultaneous operation in ZV and conventional PCMCIA modes places some restrictions on addressing. In ZV mode, use of only 4 address bits limits direct addressing to 16 bytes, but auto-incrementing pointer registers allow wider, indirect addressing.

ICs that implement ZV are in development and are scheduled for sampling within the next three months. In one collaborative effort, Databook, a developer of PCMCIA socket-controller ICs and system software, is working with Chips & Technologies (C&T), the market leader in flat-panel controllers. Databook is developing the TCIC-3 series of ZV-capable socket-controller ICs; C&T is developing a display chip that includes both video capability and a ZV port. The two companies will jointly market the new components.—by Gary Legg

Chips & Technologies, San Jose, CA. (408) 434-0600. **Circle No. 458**

Databook Inc, Ithaca, NY. (716) 292-5725. **Circle No. 459**

VIDEO-COMPRESSION CHIP SET DELIVERS 8.2 BILLION INSTRUCTIONS/SEC

The Image Compression Coprocessor (ICC) and Motion Estimation Coprocessor (MEC) two-chip video-compression chip set from Array Microsystems suits a range of digital-video-compression applications. Video applications include conferencing, authoring and editing, playback, and distribution. The chip set provides a programmable video-compression processor for multimedia systems implementing the Joint Photographic

(continued on pg 24)

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CIRCLE NO. 96

Experts Group (JPEG), Moving Pictures Experts Group (MPEG) 1, and H.261 standards.

With a computing power of 8.2 billion operations/sec, the chips let you construct a multistandard, real-time, 30-frame/sec, video-compression codec. The chip set can also quickly switch compression algorithms. The devices store input, output, and scratchpad images in DRAMs or VRAMs connected to video buses. For example, with 12 Mbits of memory, the chip set supports JPEG encoding or decoding of full-resolution CCIR-601 (720×480-pixel) images, simultaneous H.261 encoding and decoding of CIF (352×288-pixel) images, or full MPEG 1 encoding and decoding of SIF (352×240-pixel) images, all at 30 frames/sec.

The chip sets employ the company's Videoflow vector data-flow architecture, which differs from μP-style, program-counter-based designs. The architecture simultaneously controls multiple asynchronous processors and uses multiple processing units that connect through a global bus. A data-flow controller controls the global bus via simple vector instructions. Vector instructions also allow you to write programs in days.

Software- and hardware-development tools are available for the ICC/MEC chip set. The a77800 software support tools for digital-video applications comprise a Unix-based flow-graph editor, an ICC/MEC simulator, an assembler/linker, video-analysis utilities, and a C-compiler for the onboard RISC engine in the MEC. The C compiler lets programmers create their own motion-search algorithms. The software tools come with baseline programs, which users can modify, for encoding and decoding of MPEG, motion-JPEG, and H.261 algorithms.

The a77500 hardware tool comprises a VESA/ISA bus-expansion-slot demonstration board with National TV Systems Committee and phase-alternation-line video inputs and outputs. The board implements real-time encoding and decoding of all algorithms by using the ICC/MEC chip set. The a77800 software tools and a77500 demonstration tool cost $9500 each or $14,950 for both. The chip set costs $150 (OEM).—by John Gallant

Array Microsystems, Los Gatos, CA. (408) 399-1505.

Circle No. 460

Core-logic chip set for high-performance workstations

Acer Laboratories has introduced a family of core-logic chips for servers and workstations that use the Pentium, K5, or M1 μPs. The Genie chip set suits multiprocessor applications on file servers and high-performance workstations. It uses the MESI cache protocol, integrated ECC, and optimized I/O.

The Genie's 1600 core-logic chip set comprises three highly integrated chips that use an architecture that balances I/O and CPU performance for high throughput. The chip set features a 264-Mbyte/sec memory bandwidth and as much as 1-Gbyte direct-memory addressing. Although designed for high-end workstations and servers, the device also works in Windows 95 desktop workstations or dual-processor workstations for Windows NT and OS/2.

The heart of the chip set is the company's 64-bit, concurrent, performance-enhanced I/O and CPU architecture (PICA). The architecture allows for concurrency between all CPUs and Peripheral Component Interconnect (PCI) I/O devices, allowing system throughput to increase linearly as CPU performance increases. On-chip ECC provides memory protection.

The M1601 MESI cache controller supports single or multiple processors. The controller integrates a processor-bus controller, a dual-port tag RAM, a Level 2 MESI cache controller, a high-speed buffer, a host-memory arbiter, and a host-bus controller. True bus concurrency achieves a balanced performance between the processor subsystem and the I/O subsystem.

The M1609 provides DRAM control and PCI bus bridge functions. The M1609 integrates a DRAM controller; ECC/parity circuits; an I/O controller; a 256-byte, write-back I/O cache; PCI bus-interface circuits; and memory-bus circuits.

The M1513 ISA/PCI interface controller includes an integrated bus controller, a PCI prefetch, and an on-chip PCI bus arbiter with fixed or rotating priority schemes. For EISA applications, the Genie can use an external EISA chip instead of the M1513. The three-chip set costs $55 (1000/month).

—by John Gallant

Acer Laboratories Inc, San Jose, CA. (408) 433-4950.

Circle No. 461

CALENDAR OF UPCOMING EVENTS...

June 27 to 29
VMIC Conference, Santa Clara, CA, covers conductor and dielectric systems and parasitic and noise evaluations. Dr Thomas Wade, University of South Florida, Tampa, FL. (813) 974-4779.

July 10 to 14
'95 Practical Aspects of Analog and Mixed-Mode Design, Portland, OR. This five-day intensive course focuses on the practical aspects of modern analog and mixed-mode IC-design techniques and systems. Topics include transistor-level circuit design, circuit-design methods, and shielding techniques for analog and mixed-mode ICs. Oregon Center for Advanced Technology Education, Beaverton, OR. (503) 690-1460.

BURR - BROWN®

UPDATE

Low Cost Plus Low Power *SpeedPLUS* Op Amps

OPA650 and **OPA2650** are single and dual ***Speed****PLUS*, unity gain, voltage feedback op amps. **OPA650,** the single, delivers 560MHz bandwidth and a 12-bit settling time of 20ns, while only dissipating 50mW of power. Both operate on ±5V and +10V supplies.

OPA650 and **OPA2650**'s voltage feedback design offers a true differential input stage—ideal for easy implementation—for all amplifier, differential amplifier and active filter designs. And, their high speed, low power, and low cost make them ideal for video, medical imaging, communications, and portable applications.

OPA650 and **OPA2650** come in 8-pin DIP and SOIC packages and are specified over the –40/+85°C temperature range.

OPA650 key specifications:

Power dissipation	50mW
Bandwidth	560MHz
Harmonics	–77dBc at 5MHz
Settling time	20ns to 0.01%
Input bias current	5µA
Differential gain/phase error	0.01%/0.03°

OPA650 is priced from **$1.95** in 1000s; **OPA2650** from **$3.45.**

Circle No. 205

World's First Dual Instrumentation Amp

INA2128 is the first dual instrumentation amp—each comprised of three precision op amps and laser-trimmed resistors—all on a single chip. It's a low power, general purpose IA that delivers excellent accuracy.

Saves Space, Power, and $$$

INA2128 saves space, power, money…and most importantly, your time. It operates from power supplies of ±2.25V to ±18V and total quiescent current is only 1.2mA—ideal for battery operated systems. Internal input over-voltage protection withstands up to ±40V without damage. Gain of each amp is set from 1 to 10,000 with a single external resistor. With two IAs in a "space saving" 16-pin DIP or SOL-16 surface-mount package, it's an unbeatable choice for multi-channel signal acquisition applications. **INA2128** is available in 16-pin DIP and SOL-16 surface-mount packages and specified for the –40/+85°C temperature range.

INA2128 key specifications:

Offset voltage	50µV max
Drift	0.5µV/°C max
Input bias current	5nA max
Bandwidth	700kHz (G=10)
Power supply	±2.25V to ±18V
Quiescent current	1.2mA

INA2128 is priced from **$6.40** in 1000s **Circle No. 206**

Multiple Channel Signal Acquisition

New High Speed Programmable Gain Amplifiers

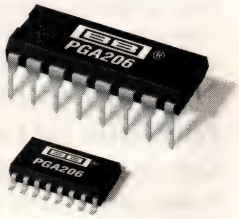
PGA206 and **PGA207** are precision, monolithic, digitally controlled instrumentation amplifiers. **PGA206** digitally selects gains of 1, 2, 4, 8V/V; **PGA207** has gains of 1, 2, 5, 10V/V. Both are ideally suited for multiplexed-input data acquisition systems.

Fast and Accurate

PGA206 and **PGA207** give you what you need—speed and accuracy. Their settling time of 3.5µs to 0.01% allows fast multiplexing of many channels, while gains are accurate to 0.05%. FET inputs eliminate errors due to multiplexer series resistance. And, they're cheaper and easier to design-in than "do-it-yourself" circuits. **PGA206** and **PGA207** are available in 16-pin DIP and SOL-16 surface-mount packages.

PGA206/PGA207 key specifications: **Circle No. 207**

Settling time	3.5µs (0.01% all gains)
Digitally programmable gain	
PGA206	1, 2, 4, 8V/V
PGA207	1, 2, 5, 10V/V
Nonlinearity	0.002%
Input bias current	100pA
Offset voltage	1.5mV (all gains)



PGA206 and **PGA207** are priced from **$8.90** in 1000s

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Isolated Differential Bus Transceiver is RS-485/RS-422 Compatible

ISO485 is a differential isolated bus transceiver that uses capacitively-coupled isolation technology to achieve high speed and low cost bus isolation. Designed for bi-directional data communication on multi-point bus transmission lines, it meets EIA standard RS-485 and RS-422 requirements. Its capacitive isolation barrier, capable of withstanding 1500Vrms, greatly reduces current spikes and makes **ISO485** ideal for use on long bus lines in noisy environments.

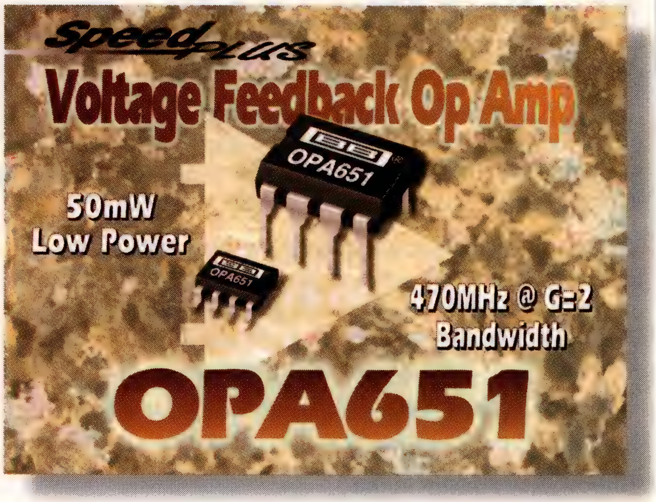
Simple and Easy

ISO485 eliminates the need for high current-consuming opto-coupler solutions, and simplifies connection to an RS-485 bus by using a single device. **ISO485**'s 3-state differential line driver and differential-input line receiver both operate from a single 5V power supply. **ISO485** is available in a single-wide 24-pin DIP and is specified over the –40/+85°C temperature range.

ISO485 key specifications:

Power	180mW typ (5Mbits/s)
Isolation voltage	1500Vrms
Data rate	35Mbits/s

ISO485 priced from **$7.74** in 1000s. **Circle No. 208**



SpeedPLUS

Voltage Feedback Op Amp

OPA651 is a new ***Speed**PLUS*, low power, wideband voltage feedback op amp—it's decompensated for stability in gains of 2 or greater. Its low 50mW power dissipation combined with 940MHz gain bandwidth product makes **OPA651** your low cost choice for video, medical imaging, communications, multi-channel, and other high speed applications.

OPA651 is available in 8-pin DIP and SO-8 packages and is specified over the –40/+85°C temperature range.

OPA651 key specifications:

Power dissipation	50mW
Bandwidth	470MHz at G=2
Harmonics	–78dBc at 5MHz
Settling time	16ns to 0.01%
Input bias current	4µA
Differential gain/phase error	0.01%/0.025°

OPA651 is priced from **$1.95** in 1000s. **Circle No. 209**

NEW

Low Cost, 12-Bit CMOS A/D Features 600kHz Sampling

Circle No. 210

ADS7831 is the latest addition to our high performance ***ADS Family.*** It's a full-function device, complete with clock, sample/hold, +2.5V reference, parallel microprocessor interface, and three-state output drivers. **ADS7831**'s 600kHz sampling rate is ideal for the communications industry—use it in HDSL modems and cellular base stations.

Performance and Low Prices!

ADS7831 delivers outstanding performance at a low, low price. Dynamic performance is excellent, with SFDR exceeding 77dB and THD better than –77dB at 250kHz. It's also a cost effective solution for transient recorders, waveform/spectrum analyzers, and data acquisition boards. It's available in 28-pin 0.3" DIP and SOIC packages.

ADS7831 key specifications:

Sampling rate	600kHz min
SFDR	77dB
THD	–77dB
Resolution	12 bits
SINAD	69dB min
INL	±1LSB max
DNL	±1LSB max
Power dissipation	275mW max

ADS7831 is priced from **$11.90** in 1000s.

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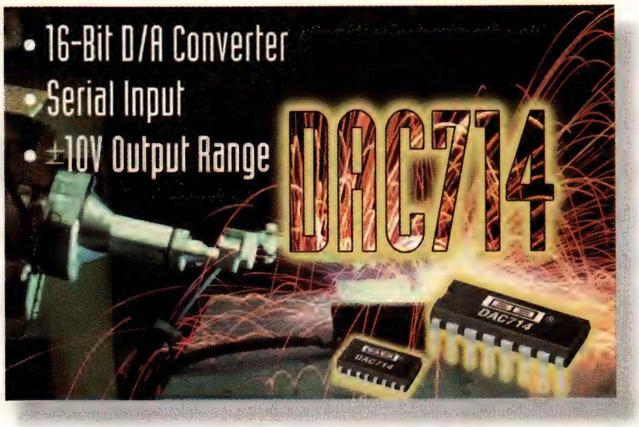


16-Bit D/A with Serial Data Interface

DAC714 is a 16-bit monolithic D/A complete with internal reference, programmable output, and serial interface. Its serial digital interface is fast, 50ns; and, it supports 100MHz data rates and serial data output for cascaded serial bus connections.

Ideal for Industrial Applications

DAC714 was designed and specified for industrial applications. It offers important advantages to customers involved with ATE equipment, analog I/O boards, robotics, process controllers, and similar designs.

Beats the Competition

DAC714 beats the competition in price, power, and package size. It's packaged in a 16-pin, "skinny" 0.3in. DIP—half the size of our competition! Power dissipation is a low 600mW, and prices are lower, too! Specified over the extended industrial temp range, it's also available in a 16-lead SOIC package.

DAC714 key specifications:

Resolution	16-bits
Settling time	10μs (max)
INL	13 bits and 14 bits
Power supply	±12V to ±15V
Power dissipation	600mW max
Voltage output	±10V

DAC714 is priced from **$13.00** in 100s. **Circle No. 211**

NEW

Precision FET-Input Op Amp Family

Our new **OPA131** family of precision, FET-input op amps delivers excellent overall performance for general purpose applications…and, for a great price, too! It features 4MHz bandwidth and 10V/μs slew rate, yet quiescent current is only 1.5mA per amplifier.

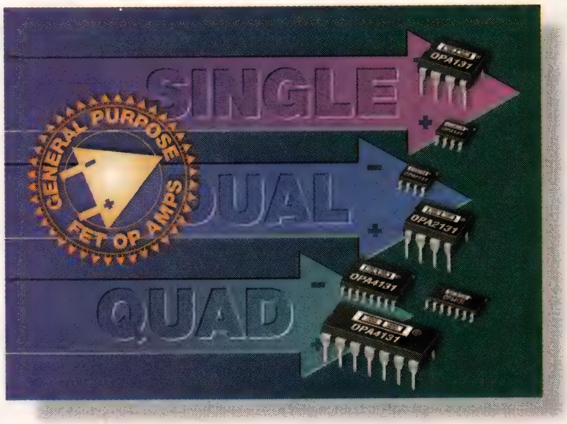
Single, Dual, or Quad Options

Available in single **(OPA131)**, dual **(OPA2131)**, and quad **(OPA4131)** versions, this innovative family supports the widest range of applications and package configurations. Package options include an 8-pin DIP and SO-8 surface mount in the single **(OPA131)** and dual **(OPA2131)**. The quad **(OPA4131)** version is available in a 14-pin DIP, SOL-16 and the smaller SO-14 surface-mount package for maximum flexibility.

OPA131 key specifications:

Input bias current	50pA max
Offset voltage	750μV max
Slew rate	10V/μs
Bandwidth	4MHz
Power supply	±4.5V to ±18V

OPA131 is priced from **$1.30** in 1000s for the single, **$2.10** for the dual, and **$3.40** for the quad. **Circle No. 212**



Audio SoundPlus ΔΣ D/A Has On-Chip Filter and Output Amplifier

PCM1715 is a low cost, dual, voltage output CMOS D/A with an on-chip filter and output amplifier. Its unique multi-level 4th-order delta-sigma architecture reduces sensitivity to input clock jitter and RF interference. The on-chip digital filter performs at 8X*f*s.

Audio and more…

PCM1715's ability to support separate L and R digital attenuators and its flexible analog output mode selection make this part your low cost solution for CD-ROM, CD-I, VIDEO-CD, tuners, set-top box, and other digital audio applications. The digital attenuator has 255 steps with provisions for separate control of Left and Right Channels making **PCM1715** compatible with the newly adopted industry-standard ATAPI (AT Attachment Packet Interface) extension for CD-ROM drive interface to PCs. And, **PCM1715**'s unique output selection possibilities—L/R reverse, mono, (L, or R, or L + R/2) or mute in addition to normal stereo mode—make it ideal for digital broadcasting applications such as set-top boxes.

PCM1715 is available in a 28-pin SOIC package and operates from a single +5V power supply. **Circle No. 213**

PCM1715 key specifications:

THD+N	–92dB
SNR	110dB
Dynamic range	98dB
Analog voltage output	3.2Vp-p

PCM1715 is priced from **$4.25** in 1000s.

BURR - BROWN®

BB UPDATE

New "femto-amp" Instrumentation Amp with 5fA Bias Current

INA116 is a complete monolithic, FET-input instrumentation amp with only 5fA input bias current. It's ideal for amplifying ion-specific electrodes such as pH probes, electric field measurement, and other ultra high impedance measurements. Use it for scientific, lab, and medical instrumentation applications.

Why Make Your Own?

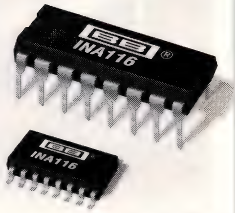
We have your perfect solution…available now. **INA116**'s guard pins adjacent to each input terminal make it easy to achieve ultra low leakage on a circuit board—even with the surface mount version. It's your "easiest" way to achieve ultra low input-bias current. **INA116** is available in 16-pin DIP and SOL-16 surface-mount packages and specified for the –40/+85°C temperature range. **Circle No. 214**

INA116 key specifications:

Input bias current .... 5fA, 25fA max
Offset voltage .... 2mV max
Drift .... 10µV/°C
CMR .... 94dB (G=100)
Power supply .... ±4.5V to ±18V
Quiescent current 1mA

INA116 is priced from **$6.95** in 1000s

INA116



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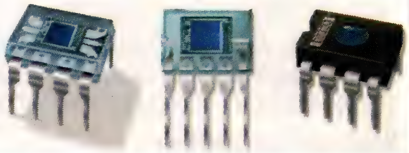

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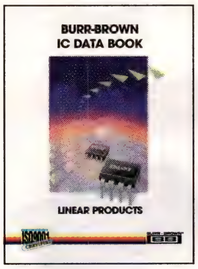

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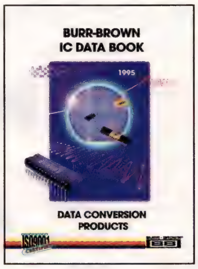

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Reader recommends trip to doughnut shop

I'd like to hear more from Do-While Jones and David Scott, author and contributor, respectively, of "Quaternions quickly transform coordinates without error buildup" (*EDN*, March 2, 1995, pg 95) on the subject of dividing by zero. On pg 96, in the equation of temporary variable TK, the author states that TK=2/(TQ+TX+Q1*Q1). Jones also states that TK=0 if (TQ+TX+Q1*Q1)=0 as a special case. This is "divide by zero," which is assigned to the value of infinity in many math texts. It is also the accepted mathematical dogma on the subject. How do the author and contributor justify their decision to arbitrarily assign this quantity with the number zero? I am curious.

Also, consider the possibility that 2/0=2. In general, if a number X is not imaginary, then X/0=X. Proof of this is the doughnut theory, which is as follows:

To perform this experiment at home, the engineer needs a bag of doughnuts and a short knife. The idea is to form a physical basis for this concept of division. This is appropriate since the resulting quaternions are said to allow meaningful rotation of physical object models. Each doughnut represents a number of arbitrary size. The number is to be divided by a smaller number, represented by the short knife, which is about half as long as the major diameter of the doughnut. As a physical model of mathematical division, this experiment involves cutting the doughnut with the knife. To represent division by two, pick up the knife. Select a new doughnut. Cut it once on the major diameter, then walk halfway around it and cut again on the other side of the major diameter. If the cutting is done very carefully, then two equal halves of doughnut result. The doughnut may be cut any number of times to represent division by any number.

Select a new doughnut; cut five times to divide by five, which results in five pieces of a doughnut, or fifths. Select another doughnut; cut four times to divide by four, which results in four pieces, or fourths. Select another doughnut; cut three times to divide by three, which results in thirds. And, select a new doughnut, cutting it into two pieces, resulting in halves. Now select another doughnut, cut one time to divide by one, which results in one piece of doughnut. It is no longer a doughnut, since the dough does not completely surround the center after this division. The doughnut resembles a torus with a gap, which resembles the letter C. It is no longer a unit doughnut after division by one. This is the first major point of doughnut theory: Dividing by one causes a mathematical change. Dividing a unit by one changes the unit.

When we divide by one, we are dividing by a unit of what? The result of division by one is dependent on the unit of division. A doughnut divided by one short knife, or divided by one brick, is one piece of a doughnut.

Here is the second major point of doughnut theory, which pertains directly to the equation of variable TK in the "Quaternions" article. Select a new doughnut. Pick up the knife. Divide the doughnut by zero. That is, do not touch the doughnut. Put the knife down. The doughnut has been divided by zero. Let's look at the results of dividing by zero.

After the doughnut has been divided by zero, are there suddenly an infinite number of them? No. This result is patently absurd. Therefore, most mathematical textbooks are wrong. Dividing a number by zero does not result in infinity.

After the doughnut has been divided by zero, does it disappear? Are there suddenly zero doughnuts to be seen? Once again, no. Mr Jones and Mr Scott may have erred on this seemingly minor point. Dividing a number by zero does not result in zero.

How many unit doughnuts result from dividing a unit doughnut by zero? One. A unit. Therefore, when (TQ+TX+Q1*Q1)=0 then TK=2/(TQ+TX=Q1*Q1)=2. QED.

This proof of divide by zero, which uses a physical model of a doughnut divided by a knife, is not dependent on the actual size of the knife.

Now, go ahead, destroy the evidence—eat the doughnuts!

Michael Klaus
Glendora, CA

Ed note: *If you look at the definitions for TQ and TX, you'll see that TQ+TX+Q1*Q1 is really* $Q1^2+Q2^2+Q3^2+Q4^2$. *The only way for the sum of four squares to be zero is if all the terms are zero (which is not a legal quaternion, so it should never happen). The ancient version of Fortran Mr Scott used when he wrote the algorithm did strange things when it divided by zero. He assigned 0 to TK to make the routine return a benign identify matrix for this pathological, impossible case.*

Several other readers wrote concerning algorithm 2 (pg 98). Unfortunately, the "<" signs all evaporated during typesetting. The four cases should have read:

$\text{if } M11\geq 0 \text{ and } (M22+M33)\geq 0$
$\text{if } M11\geq 0 \text{ and } (M22+M33)<0$
$\text{if } M11<0 \text{ and } (M22-M33)\geq 0$
$\text{if } M11<0 \text{ and } (M22-M33)<0.$

No one wrote to question an apparent polarity problem. For reasons I don't care to defend, it has always been the practice where I work that the ground-referenced coordinate system is East/North/Up, and the airframe-referenced systems are North/East/Down. Long ago, I incorporated a change in order and polarity of axes into the quaternion/matrix conversions to take this into account. I had forgotten that I hid this little trick in the conversion algorithm. I regret not mentioning this in my article and hope it caused little inconvenience.

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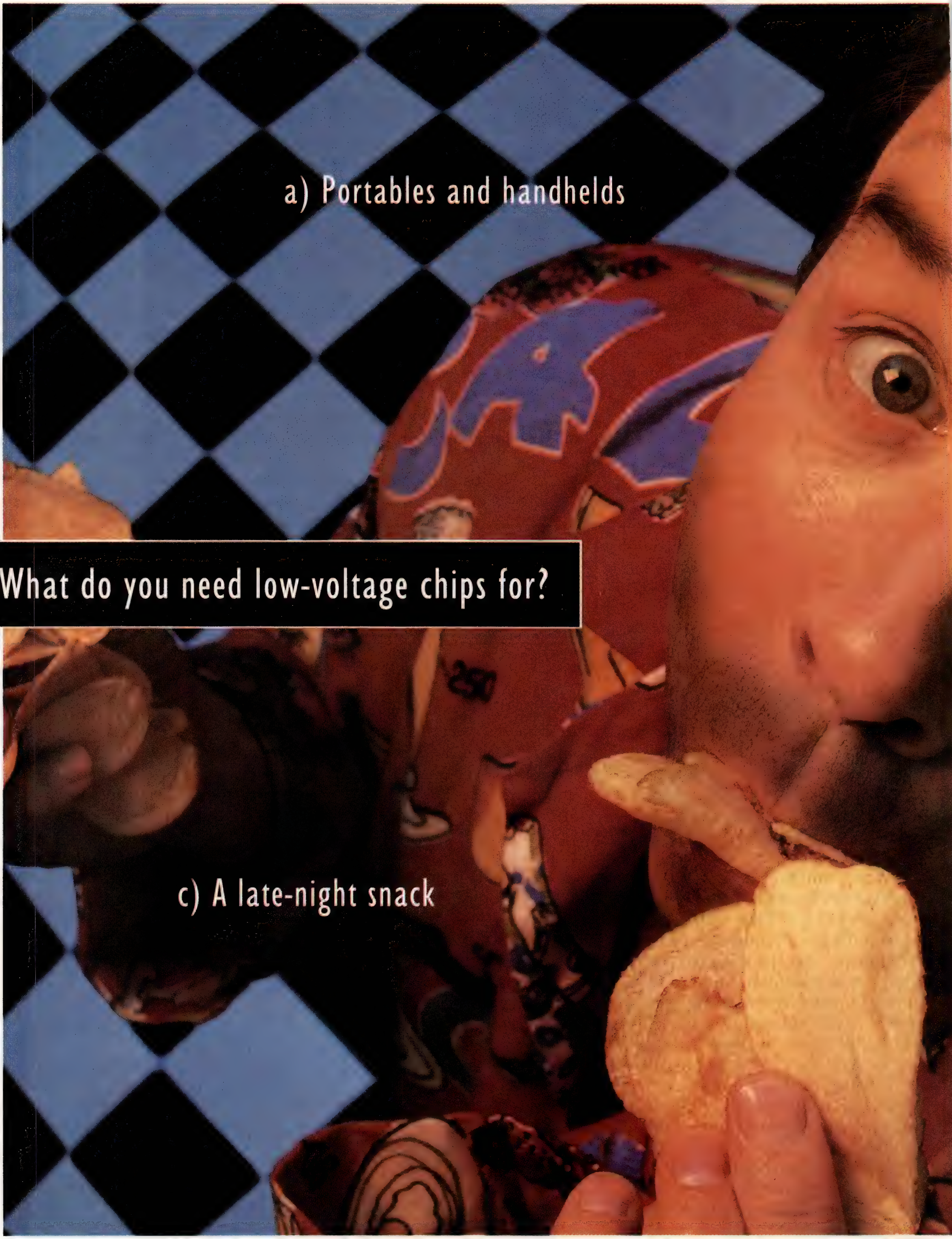

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x86-processor derivatives have become so abundant that system developers must invest large amounts of time to determine which works best for their embedded PC. Key decision-making factors include cost, performance, longevity, and the degree of CPU integration.

Photo courtesy Intel Corp
Photography by Richard Wahlstrom Photography Inc

ZERO IN ON x86 DERIVATIVES FOR YOUR EMBEDDED PC

MARKUS LEVY, TECHNICAL EDITOR

System designers use x86 processors in an endless variety of applications, including industrial controllers, robotics, network controllers (bridgers and routers), handheld inventory devices, hard-disk controllers, security systems, in-flight-phone and -entertainment systems, and even ice-cream dispensers. System designers have long understood the benefits of PC compatibility in an embedded system; however, there are now many complex issues involved in selecting an x86 CPU.

No other computer architecture has evolved as wide an assortment of assemblers, compilers, debuggers, simulators, operating systems (OSs), and applications as has the x86. Some companies even have products that do not require PC compatibility but still use an x86 processor to maintain OS and application-software homogeneity across product lines. An x86 processor leverages the competitive pricing of the desktop PC market, a benefit equally as important as compatibility. On the other hand, system designers are finding it difficult to keep pace with the desktop PC market, making your CPU choice critical to the longevity of your product.

What's an embedded PC?

Engineers often refer to an x86-based application as an embedded PC, even if it only remotely resembles a PC. But, an embedded PC is really a feature, or a component, of an application—not a market segment. From a functional standpoint, an embedded PC provides standardized mechanisms for inputting and displaying data as well as the ability to provide hardware and software flexibility. Most important, by treating an embedded PC as a component, you stay focused on your product's value-added software or hardware elements.

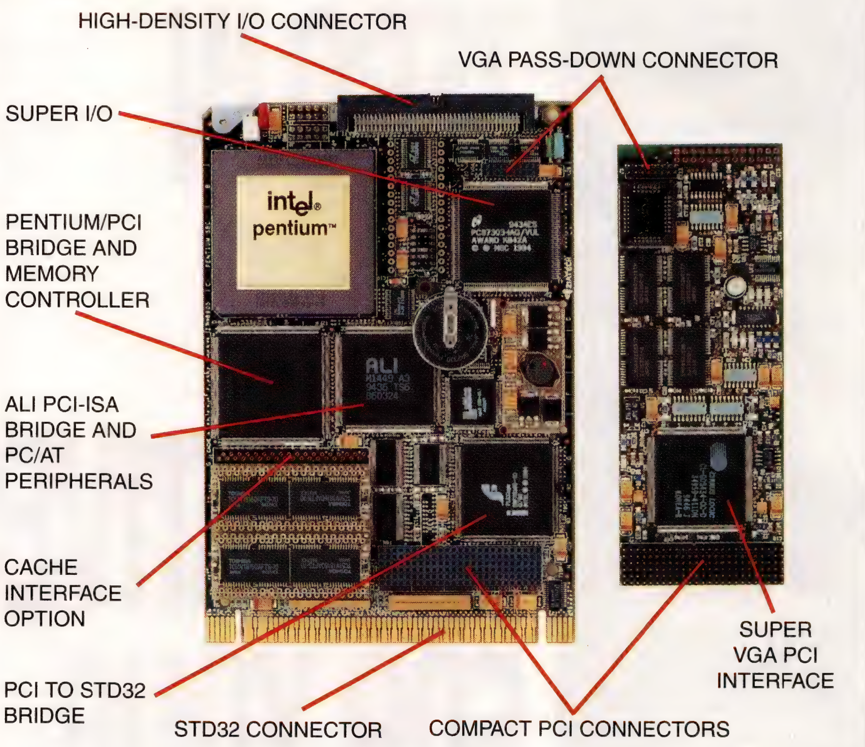
This last point begs the question of whether you should build or buy your product's embedded-PC component. Beginning with the introduction of the 386, the CPU market evolved rapidly. At that point, many OEMs began buying embedded PCs instead of redesigning with a new CPU or chip set every six to 18 months. This trend has continued, suggesting that an increasing number of embedded-system developers are opting not to reinvent the wheel. Furthermore, by purchasing the embedded PC for your system, you won't have to worry about understanding the hardware idiosyncrasies and compatibility issues of standard desktop PCs.

On the other hand, if you build your own embedded PC, you have the opportunity to choose the exact peripheral functions needed. An off-the-shelf single-board computer (SBC) may contain more features than your design requires. (It may still be less expensive by the time you add in design and manufacturing costs.) For example, to offer a compromise, Dovatron International manufactures modular SBCs that plug into a card cage. You can add features by plugging in additional modules such as VGA, PCMCIA, Ethernet, SCSI, etc. Alternatively, Radisys Corp offers PC-compatible boards but specializes in providing custom solutions to allow you to add (or remove) special features.

Before embedding a PC into your product, you have to interpret different degrees of PC compatibility. Some designers maintain that if the embedded PC runs x86 code, it's PC compatible. Others stretch it a little further, saying that, as long as it runs "well-behaved" DOS and Windows applications, it's PC compatible. Still other designers say that, to be PC compatible, the embedded PC must support the complete PC-AT specification, including all ISA bus signals. The processor (and core-logic chip set) you choose determines how PC compatible your embedded PC can be.

The definition boils down to determining what features you really need to support: a monitor, a keyboard, a floppy or hard disk? What about ISA bus add-in cards? All of these are basic PC features. How about adding nonstandard features (common in embedded PCs) such as solid-state disks or extra RS-232C ports? Again, the processor you choose affects how easily you can accommodate these features.

FIGURE 1



The ZT 8905 SBC from Ziatech Corp demonstrates the complex board layout required for a Pentium-based design. Although the board measures just 4.5×6.5 in., it is 100% PC-AT compatible and includes both PCI and STD32 interfaces.

Select the right processor

One of the first steps you must take in selecting an x86 processor is determining the processing power your application requires. You can find non-x86 processors that deliver higher performance than any x86 processor, but x86 processors have a guaranteed upgrade path (due to the desktop PC market) and double their performance every 18 months. And, even though 186s and 286s may provide ample performance for many applications, the trend appears to be following the rapid pace of desktop PCs, where 486s represent the performance entry point. This trend is carrying over to the embedded market (typically lagging by a minimum of two years): 386s, 486s, and Pentiums are becoming increasingly popular for performance-demanding functions such as enhanced graphical user interfaces.

If your application needs performance at the upper-most end of the x86 spectrum, the choices are simple. You can select from 586-class processors that include Intel's Pentium, AMD's K5, Cyrix's M1, or maybe even Nexgen's 586. When combined with the supporting core-logic chip set, these CPUs allow you to build any degree of PC compatibility. The Pentium, K5, and M1 share the same pinout, theoretically making it possible for the chip sets (available from a multitude of vendors) to work with any of these CPUs. Because 586-class CPUs are at the leading edge of performance, you are almost guaranteed product availability for several years. However, the same guarantee may not be the case with chip sets that seem to change every six months. The unique pinout of Nexgen's 586 amplifies the instability of chip-set support; as a result, it may be even more difficult to maintain an embedded-PC design.

Although the choices are simple for the 586-class CPUs (because there aren't many), it's the system layout that presents a challenge. This situation is especially true if you're designing a small form-factor board, as is typically the case for embedded PCs. Ziatech Corp's STD32-bus-based ZT 8905 SBC exemplifies this situation (**Fig 1**). This Pentium computer board is made 100% PC-AT compatible by using Acer Labs Inc's (ALI's) Aladdin PCI M1511/M1513 core-logic chip set ($22 each). Ziatech chose the Aladdin because the implementation only requires two devices, which is essential for squeezing an entire Pentium computer on a 4.5×6.5-in. board. However, in order to get away with only two devices, ALI's 1461 DRAM controller doesn't include on-chip drivers. Thus, the multiplexed address and data buses for the DRAM interface require external drivers (245s). The additional cost for the drivers is sometimes a problem for penny-pinching desktop PCs. Designers at Ziatech benefited from ALI's chip set by putting the drivers on the back side of the board using 17 TSOPs.

An abundance of 486s

The 486-class CPUs offer many more options for building an embedded PC when compared with 586-class CPUs. Different versions of the 486 are manufactured by a long list of companies, including Intel, AMD, Cyrix, Texas Instruments, IBM Microelectronics, and SGS-Thomson. Amazingly, the 486 has become a commodity product, but this helps to ensure its longevity, and it continues to drive down prices.

The 486-class CPUs consist of 16- and 32-bit versions. The 32-bit versions include the SX (with no floating-point unit), DX2, and DX4 processors. The 486 CPUs, such as the 486SLC from Cyrix and TI, have a 16-bit bus interface that allows you to drop it into a 386SX socket. The 32-bit versions have the widest range of support from CPU and chip-set vendors. Incidentally, Intel and AMD are supporting 486s as embedded processors, indicating a commitment to product longevity and the enlistment of chip-set vendors such as PicoPower, ACC Micro, and Intel. AMD's 486SE, identical to a 486SX, is an embedded CPU (from a company-support standpoint). PicoPower's Pine core-logic chip set ($22) supports all 32-bit CPUs (386s and 486s), making it easier for the company to leverage manufacturing efforts. Also, because Pine supports both 386 and 486 CPUs, it minimizes your efforts for redesigning the hardware and BIOS when upgrading.

When it's actually time to make a selection, embedded-PC designers find that the 386 class generates the most confusion. The 386 has virtually left the desktop PC. Devices such as the 386SX and 386DX are supported almost exclusively as embedded products. As a result, chip-set support has all but disappeared, with only a few vendors—Chips and Technologies, ALI, and PicoPower—still actively supporting these CPUs.

Similar to the SE device in the 486 category are the 386SE and 386DE, which AMD markets for embedded applications. The SE and DE, however, differ a bit from their SX and DX counterparts. Specifically, the SE and DE have had their paging units removed to help reduce cost. The 386SE ($10.50) and 386DE ($12) each cost about $0.25 less than their 386SX and 386DX counterparts, respectively. But, without the paging unit, you give up the ability to run Windows. Chips and Technologies' CS4031EM Chipset ($15.65) and the 82C836EM "SCATsx" system logic chip sets support SE and DE devices (as well as SX and DX devices). The company has agreed to support these chip sets for at least four years.

About a year and a half ago, Intel introduced a 386 specifically targeted at embedded PCs. This device, the 386EX, contains a 386 static core surrounded by a set of almost-PC-compatible peripherals that include DMA and interrupt controllers, serial ports, a parallel port (not EPP compatible), watchdog timer, timer control unit, and refresh unit. These peripherals lessen your dependency on a potentially volatile chip set. Additional benefits of using a highly integrated CPU include higher system reliability, better power management, and smaller board space. The 386EX carries a price tag of $24, which is reasonable if you consider the range of peripherals on this device. But, before you buy a 386EX-based SBC or begin developing with the EX, decide on the degree of PC compatibility your product requires.

The 386EX includes dual 8259A-compatible interrupt controllers (PC compatible). Pin-count limitations forced Intel not to connect IRQ10, IRQ11, and IRQ15 to external pins. Although these IRQs are unassigned ISA bus interrupts, they are required for ISA bus compatibility. You may decide on a partial ISA bus implementation using add-in cards that do not require these interrupts. Or, more than likely, your embedded PC doesn't support add-in cards anyway.

A partial solution to the interrupt-pin shortage is to utilize some of the other available interrupts. For example, if you aren't using a numeric coprocessor, you can reassign IRQ13, which normally is used by the coprocessor for signaling an error. Likewise, a system without a hard drive can reassign IRQ14. However, reassigning IRQs may not solve this problem because ISA add-in card's hardware may not allow the IRQs to be steered to these interrupt lines.

No floppy disk?

PC-AT compatibles have eight DMA channels; the 386EX has only two. Specifically, the EX supports DMA channels 0 and 1. On PC-AT compatibles, channels 0 and 1 are assigned to memory refresh and serial communi-

LOOKING AHEAD

Applications that use an embedded PC should grow from 20 to 34% within the next two years (**Ref 1**). Also, note that among the OEMs using embedded PCs today, 48% of these OEMs are building their own, but this number is expected to drop to 38% within two years. In response to this tremendous growth, vendors supporting embedded PCs, that is, CPU and chip-set vendors, will offer more products with increased longevity.

Later this year, National Semiconductor will join the fold of vendors supporting embedded PCs. National plans to produce a sole-sourced device that will contain a 486 core surrounded by integrated peripherals, a move intended to help decrease system costs. These peripherals will include a DMA controller, PCMCIA interface, UARTs, parallel ports, timers, and a DRAM controller. Although this CPU is not PC-AT compatible, it can still utilize the huge software base supported by the x86. It's likely that Intel and AMD soon will be developing 486 versions of the EX and Elan, respectively.

cations, respectively. Floppy disks use channel 3.

You have several choices for getting around the lack of floppy-disk support on the 386EX. The simplest solution is not to use a floppy disk, which generally isn't an issue on embedded PCs. New applications or data can be downloaded to the embedded PC using a serial or parallel connection. The 386EX has a separate refresh control unit, freeing DMA channel 0 for reassignment to a floppy disk. Alternatively, your embedded PC's BIOS can be rewritten to accommodate the redirection. As long as programs don't try to circumvent the BIOS and go directly to hardware, no problems will occur. Watch out for Windows, however, which may cheat and go directly to the floppy-disk hardware. (Windows 95 allows you to direct floppy services through the BIOS). Embedded applications that use a floppy disk use them primarily through DOS for loading new programs into the system (which always goes through the BIOS).

If you're building a "real" PC with the 386EX, you'll need to add a few more peripheral devices, such as graphics, memory controllers, a keyboard, a real-time clock, a parallel port, and perhaps circuitry to generate the ISA bus signals if you plan to support some add-in cards. The Explorer Series SBC evaluation platform, which Radisys Corp designs and manufactures for Intel, offers an example of what you can do with the 386EX (**Fig 2**). This SBC lacks an ISA bus connector but uses a synchronous expansion bus (SEB) and a digital I/O channel to access off-board peripherals. The SEB provides a subset of the ISA bus with processor-synchronous timing.

Many SBC vendors, such as Ampro and WinSystems, which have PC/104 connectors on their boards, decided that 100% PC-AT compatibility is essential. Therefore, they had to use the 386SX instead of the EX. Basically, no amount of BIOS modifications could allow vendors to deliver 100% compatibility through the PC/104 (ISA bus signals) connector. Additionally, these vendors have found that the cost of adding a CPLD (or ASIC) and other logic to an EX design to make it PC compatible is roughly equivalent to buying a CPU and core logic chip set.

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Another "almost" PC-AT-compatible CPU is AMD's Am386SC300 (commonly called Elan), which AMD originally targeted at very-high-volume handheld devices such as personal communicators. Although the 386SC300, which costs $39 for a 25-MHz version, costs 1.5 times as much as the 386EX, it's packed with twice as many peripherals. Additional peripherals include a memory controller, ISA bus controller, EPP-compatible parallel port, CGA controller, and two PCMCIA-card controllers. However, to use these peripherals, you must make trade-offs. For example, because the 386SC300 is only available in a 208-pin PQFP, the pin limitation forces the ISA bus, local bus, and CGA controllers to share the same pins. Thus, your system can only utilize one of these functions.

Elan's internal LCD controller supports CGA sizes of 320×200, 640×200, and 480×320 (predominantly flat-panel displays). Adastra Systems, an SBC manufacturer specializing in integrating flat-panel displays, has considered the Elan for an SBC. However, the company has determined that almost any design would require using an external VGA controller. Unfortunately, most of the displays Elan supports are either obsolete, not manufactured in the technology of interest (such as active-matrix color LCDs), or not readily available.

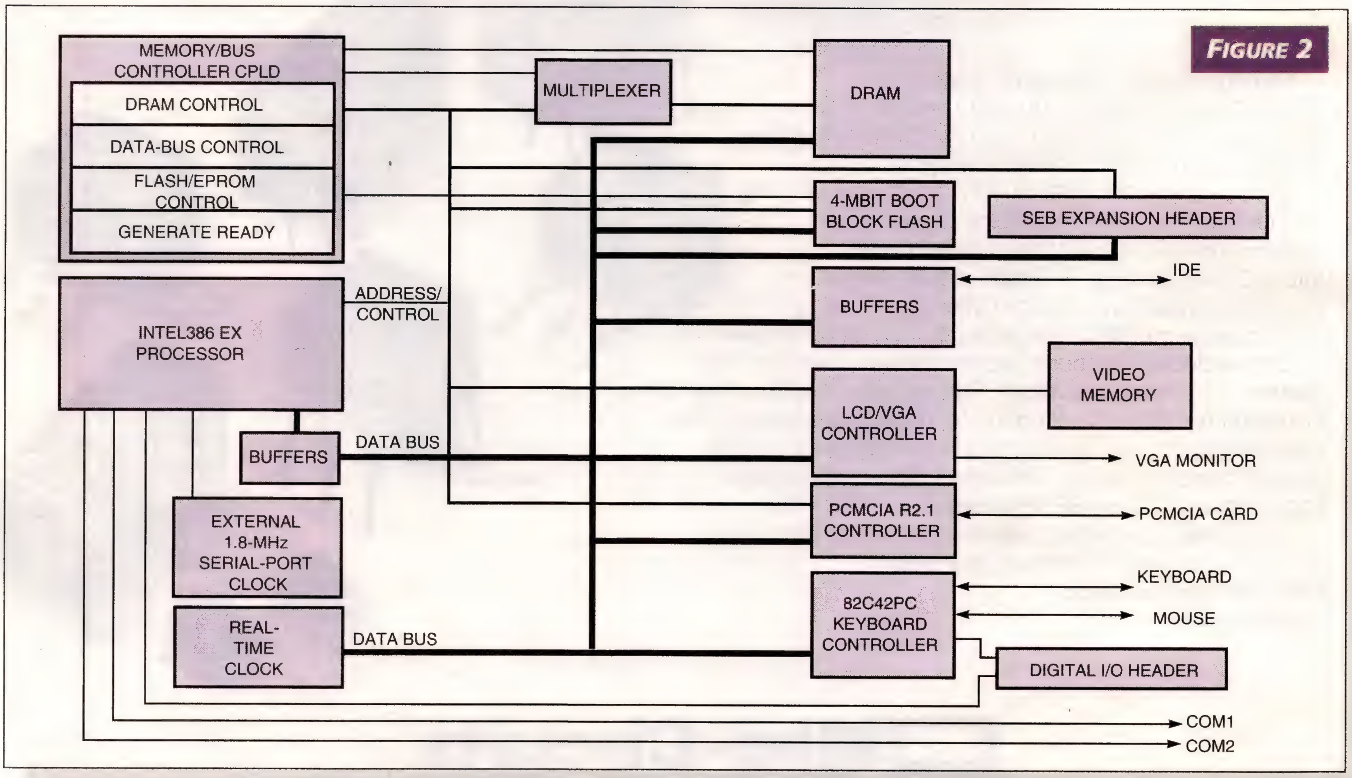
When you use the 386SC300's internal CGA controller, it supports a minimal ISA bus (this capability includes basic memory and I/O reads and writes, DMA channel 2, and a few interrupts). If you configure the 386SC300 into the local-bus mode, the internal CGA controller is disabled, and the CPU provides a few more ISA bus DMA channels and interrupts. The local-bus option basically is a 386SX local bus. The maximum ISA bus mode supplies the balance of the signals for the DMA channels, interrupts, ISA-latched addresses (LA17-LA23), zero-wait-state request, and address latch enable. Unless you plan to build a system with ISA slots, it makes the most sense to operate the Elan CPU in the local-bus mode and add an external VGA controller.

Also, when considering the 386SC-300, note that it only supports a single serial port, which may be a limitation in embedded PCs (most support at least two). Also note that, from a development/debugging standpoint, the 386SC300 lacks any type of emulator support. However, the 386SC300 is typically used in system environments similar to those of desktop PCs, where software support is almost exclusive. In this case, it may also be most appropriate to use tools such as a PROM ICE, logic analyzer, and, perhaps, a serial debugger.

A 186 upgrade path

If you're only using x86s because of software compatibility with the PC, check out AMD's 386EM, which is derived from an enhanced version of its 186EM. This non-PC-AT-compatible device provides a 32-bit upgrade path for the 186EM. Peripherals integrated into the 386EM include an interrupt controller, counter/timers, DMA controller, watchdog timer, and serial ports. AMD's 386EM sells for $24.94.

FIGURE 2



The Explorer Series SBC, which Radisys Corp designs and manufactures, runs DOS/Windows and features a 25-MHz Intel386EX. This board is available through Intel as an evaluation platform.

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Back when the first motherboards were built, chip sets consisted of discrete components such as the 8259 (interrupt controller) and 8237 (DMA controller). Today, ASIC, FPGA, and CPLD vendors are offering these components as functional system blocks (FSBs) or macrocells. You can "glue" the appropriate FSBs together to build your own integrated core logic. "Owning" the core logic puts you in better control of your embedded PC's destiny. However, you have several considerations when using this approach:

- If you're building an ASIC, production volumes must be high enough to recuperate NRE costs.
- A programmable-logic device costs four to six times more than an ASIC. For example, the CPLD used in the Radisys design (**Fig 2**) costs $30 to $50; a functionally equivalent ASIC costs $5 to $10 (not including NRE).
- The FSBs or macrocells may not be optimized for your application, potentially affecting die size (gate count) and performance.

Instead of building your own ASIC, you may be lucky enough to land an agreement with a chip-set vendor to build its discontinued devices. Be wary, however: Chip-set vendors are typically unwilling to disclose core-logic-design secrets. Alternatively, you may have the opportunity for a last-time buy, which doesn't help your inventory but outweighs the option of having to use engineering resources on a redesign.

The best thing you can do for an embedded PC is to isolate it from the rest of your application. By doing so, you won't be concerned about CPU and chip-set changes. To accomplish this, you can buy off-the-shelf SBCs and let the vendor hassle with the changes in hardware and firmware. If you're building the SBC, you may want to use an alternative approach, such as in Ziatech's ZT 8905 SBC. This SBC provides an interface to the STD32 bus. Ziatech has painstakingly developed a custom interface between the PCI bus (generated by the ALI chip set) and the STD32 bus. Even if the chip set or CPU changes, PCI bus standardization ensures that Ziatech's custom interface remains unchanged. The company's biggest concern, however, is that a CPU or chip-set change may affect board layout (for example, more chips required), which, in turn, may affect how the SBC fits within their customer's original enclosure.

Don't forget BIOS support

In addition to deciding on a CPU/chip set based on performance, price, and longevity, you should also examine BIOS support. The closer your embedded PC is to its desktop-PC counterpart, the easier it will be for you to obtain an off-the-shelf BIOS.

Fortunately, BIOS vendors are beginning to appreciate the value of embedded PCs and are making it easier to modify or add to their standard BIOS offerings. For example, almost every SBC vendor provides a flash solid-state-disk option. Another example is the keyboardless BIOS, a capability requested by 50% of companies involved with embedding PCs into their products. Despite the availability of off-the-shelf BIOSs, many SBC vendors still choose to write their own BIOS, easing the move to support custom features and accommodate design changes.

CPUs such as the 386EX and 386SC300 don't transcend the desktop-PC world. A semicustom BIOS is essential when using these processors in an embedded PC. Phoenix Technologies offers a product called PhoenixPICO BIOS, which supports both CPUs. PICO lets you add nonstandard extensions, such as I/O through serial ports, different screens, or the ability to boot from a PCMCIA device. Furthermore, the PICO BIOS is "object oriented" in the sense that it's easy to build a system and then pick only the pieces you want to use.

Cost is an obvious drawback with an off-the-shelf BIOS. As with the hardware portion of an embedded PC, you have several considerations. On one side, if your product volumes are low (<1000 qty), it is probably better to buy rather than build, because you cannot justify the development costs. It took Phoenix three man years to develop BIOS support for the 386EX. However, if you're buying a custom BIOS such as the PhoenixPICO, because of NRE charges, it really isn't economical, unless you purchase at least 1000 pieces.

If you're building your own embedded PC with 386-class performance and do not need 100% PC-AT compatibility, one of the integrated CPUs from Intel or AMD is probably your best bet. You eliminate the core-logic chip set and, therefore, have better control over the longevity of your design. Integrated 486- and 586-class CPUs don't exist yet, so you'll have to use an off-the-shelf chip set with guaranteed PC-AT compatibility. Since 486- and 586-class CPUs are mainstream today, you are guaranteed product availability for at least a few years. Regardless of how you slice it, there are no clear-cut answers for making the "right" CPU choice for an embedded PC. But, fully understanding all of your options should be the first step in making your task a bit easier. EDN

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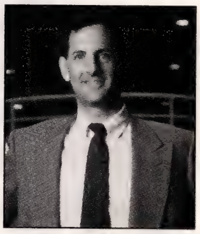

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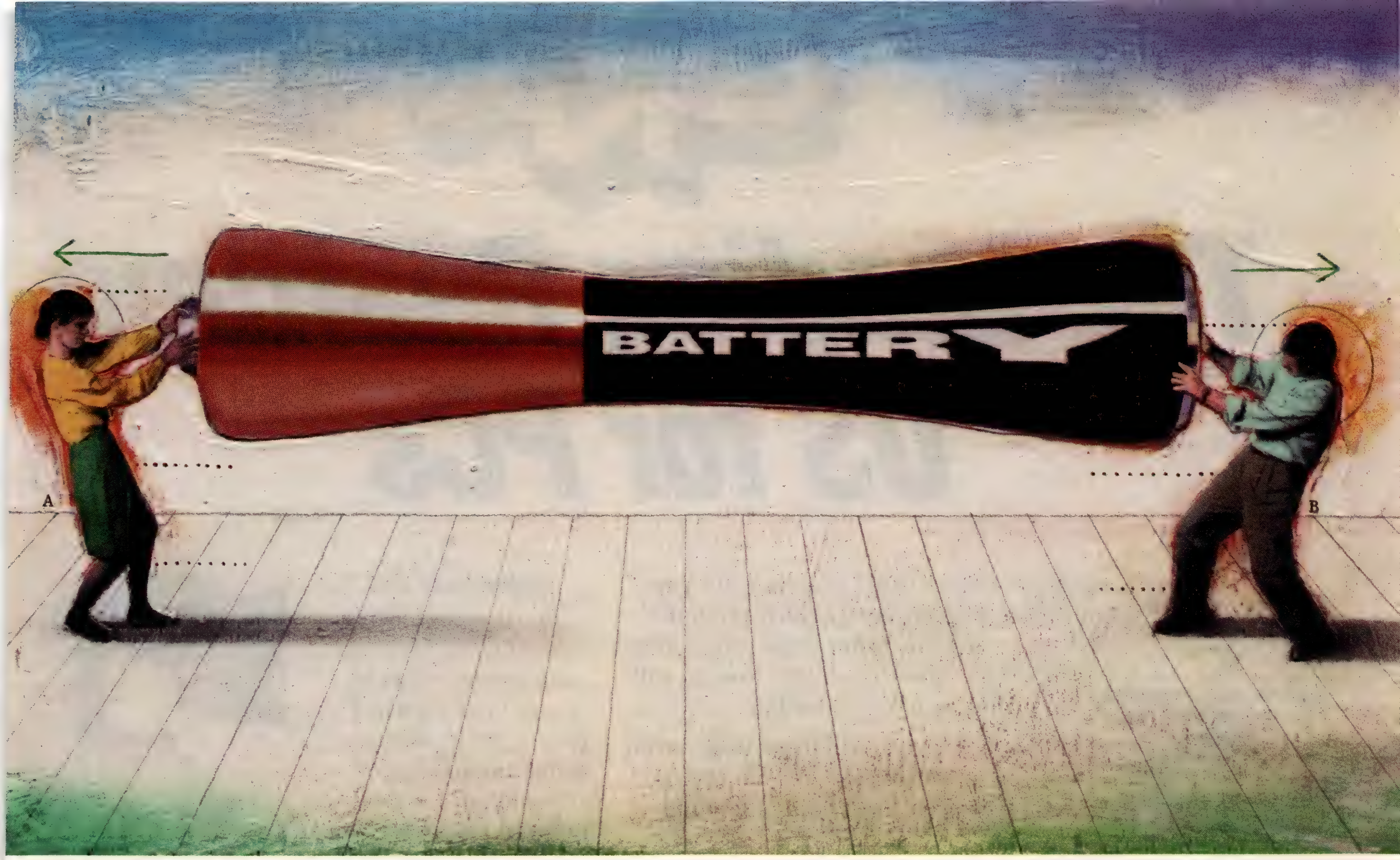

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CIRCLE NO. 123

SMART-SENSOR STANDARD WILL EASE NETWORKING WOES

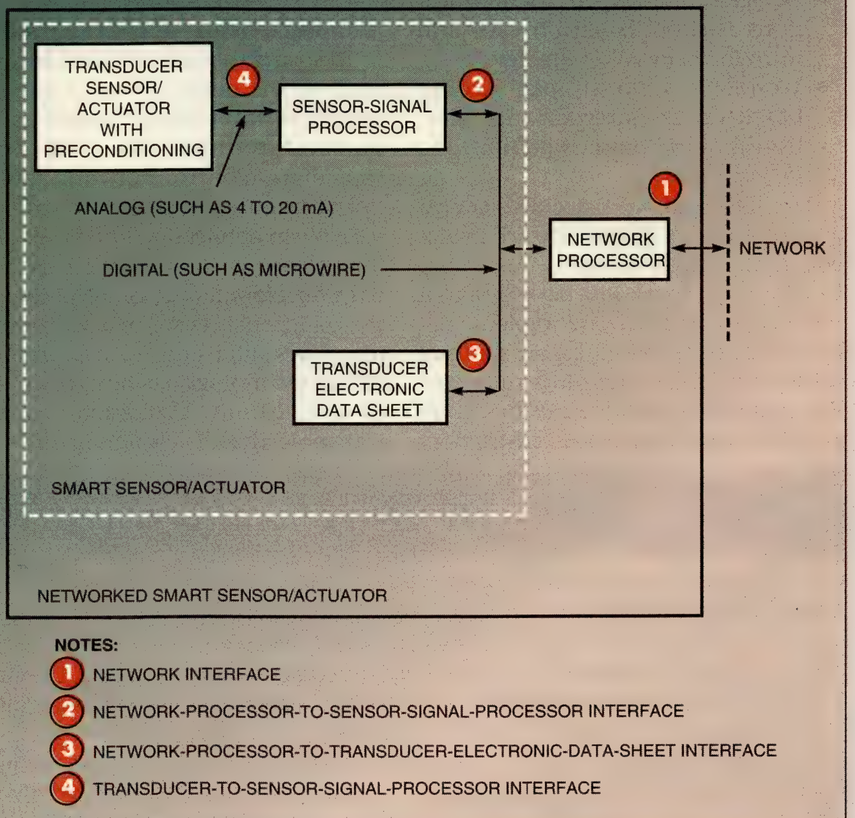
BILL TRAVIS, SENIOR TECHNICAL EDITOR

An upcoming hardware-independent, smart-sensor interface standard will allow you to connect a variety of sensors to multiple networks.

For anyone attempting to choose a sensor-interface or -networking standard, the range of choices is overwhelming. Some standards are open, and some are proprietary to a company's control products. To remedy the situation, the IEEE and the National Institute of Standards and Technology (NIST) are developing the IEEE TC-9 Smart-Sensor Communication Standard. The standard, which is due at year's end, will unite the fragmented sensor market.

The sensor market comprises widely disparate sensor types (see Question 4 in the questionnaire on pg 54). Designers consume relatively large amounts of all types of sensors. However, the lack of a universal interface standard impedes the incorporation of "smart" features, such as an on-board electronic data sheet, onboard A/D conversion, signal conditioning, device-type identification, and communications hand-

FIGURE 1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① NETWORK INTERFACE
② NETWORK-PROCESSOR-TO-SENSOR-SIGNAL-PROCESSOR INTERFACE
③ NETWORK-PROCESSOR-TO-TRANSDUCER-ELECTRONIC-DATA-SHEET INTERFACE
④ TRANSDUCER-TO-SENSOR-SIGNAL-PROCESSOR INTERFACE

The proposed functional diagram of the networked smart sensor/actuator shows levels for possible standardization of the interface.

shaking circuitry, into the sensors.

A universally accepted sensor-interface standard will not only allow for the development of smarter sensors but also lead to lower expenses because it costs less to design to a single standard. To develop the new standard, the IEEE and NIST considered the pros and cons of the following standards at a smart-sensor workshop in March 1994:

- InterOperable Systems Project (ISP)—a merging of the ISP SP-50 Fieldbus physical layer with the German Profibus and French Factory Implementation Protocol (FIP) data-link and application layers
- Controller-Area Network (CAN)—a message-based networking system for the automotive industry
- LonWorks—an open networking system introduced by Echelon Corp
- J1850—an automotive networking standard approved by the Society of Automotive Engineers
- DeviceNet—an open communications network based on CAN and introduced by Allen-Bradley
- WorldFIP—a global open fieldbus based on an International Electrotechnical Commission (IEC) and ISA standard.

The IEEE and NIST decided against adopting one of these network protocols as the single standard. According to the study, users will have different preferences for hardware implementations because of the emerging status of the low-cost smart-transducer industry. For some designers the sensor's compatibility with the devices' instrumentation is important. Other designers will take company alliances into account. And, still others will make choices based on personal preferences. The study concludes that standard setters can't force users to implement a specific smart-transducer protocol, especially when other system components are using different approaches (**Ref 1**).

The IEEE and NIST decided instead to develop a hardware-independent communication standard for low-cost smart sensors that includes device models and interfacing to selected low-cost networks, such as ISP, CAN, LonWorks, and J1850. The key phrase here is "hardware-independent." Designers will not have to develop smart sensors for any particular network protocol. Instead, the standard will lead to the development of a generation of smart sensors and associated network-adapter circuits that are not committed to a particular network.

A smart-sensor/actuator model

To ensure that the standard incorporates all the necessary parts, the IEEE and NIST interviewed designers and suppliers for input. The group found that many control-network applications are available, each with strengths for a given application and weaknesses for others. Each network requires a large development effort, especially by the traditional sensor or actuator manufacturers still using analog communication technology, such as 0.5 to 4.5V or 4 to 20 mA. Manufacturers can't transport the development effort to other networks. This scenario creates a major stumbling block for the manufacturers, which are typically small companies with limited R&D budgets. These companies are usually unfamiliar with sophisticated networking technology.

The IEEE and NIST aim to lower the networking entry barrier for sensors and actuators by creating the hardware-independent standard. Standardization will encompass the formation of two software models: The smart sensor/actuator model describes a standardized behavior of sensors or actuators in terms of interfacing signals, such as read/write, open/close. This model requires the presence of a standardized transducer electronic data sheet (TEDS) in a memory. The TEDS will include such information as the device model, the name of the manufacturer, the range, and the accuracy. The networked smart-sensor/actuator model maps, or translates, the network-capable application processor (NCAP) onto a specific network. The NCAP will interface with a smart-sensor/actuator model and will include application-specific software that supports the interfacing signals, such as the FFT algorithm.

The numbers in **Fig 1** represent locations for possible standardization of the proposed interface. The network interface in **Fig 1—1** takes data packets from the network processor in a form appropriate for the network. The sensor-signal processor is a type of ADC that covers the analog signal (**Fig 1—4**) from the sensor/actuator to a digital

LOOKING AHEAD

The proposed smart-sensor interface standard will provide many benefits to the industry. Sensor developers can incorporate smarts into their devices without worrying about network-protocol compatibility. Designers who integrate sensors into their factory-automation or process-control systems can count on an easier integration process. Assume, for example, a DeviceNet application needs a particular temperature sensor. Previously, a system integrator had to convert the sensor's analog output to digital form, then format the digital signals to satisfy the network protocol. With the new standard, sensor manufacturers will produce devices that have onboard A/D converters with outputs that are compatible with a variety of network processors.

The sensor-to-network-processor industry is another market that the standard will spawn. For example, a DeviceNet integrator must simply connect the sensor to the network processor, and the system is ready to go. Depending on industry usage, the temperature sensors might contain all the smarts necessary to connect them directly to DeviceNet. You can expect self-test of sensors that use the new standard and direct delivery of diagnostics information to the network.

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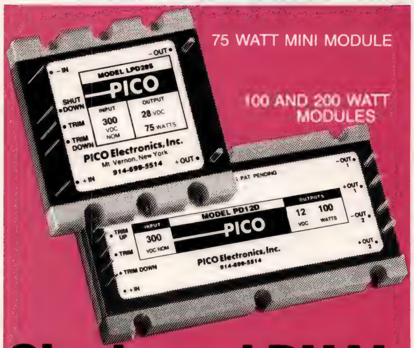

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FOR FREE INFORMATION...

For free information on the proposed smart-sensor interface standard discussed in this article, contact the following organizations directly. When you contact them, please let them know you read about their standardization project in *EDN*.

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form (Fig 1—2), suitable for network adaptation by the network processor.

As Fig 1 shows, three levels of sensor smartness, or completeness, are possible. The transducer has no smartness at all and simply translates the sensed quantity into an analog signal. The smart sensor/actuator has onboard A/D conversion and an electronic data sheet. The networked smart sensor/actuator has the features of the other two and also contains the adapter, and possibly application-specific software, for the network.

Benefits to the user

A smart-sensor standard will offer compatibility with the majority of control networks suitable for analog output sensors, such as pressure sensors, and actuators, such as proportional valve. The standard will eliminate the need to develop new network hardware, allowing you to develop standardized software. You can easily transport this software to different networks. The development effort to produce the first network interface for the analog-output sensors/actuators will drop by about 50%. This drop will result in a 90% reduction in the development effort for subsequent network interfaces for the same sensors/actuators. The standard will also establish plug-and-play compatibility between sensors and networks, allowing interfaces of given sensors/actuators to different networks. EDN

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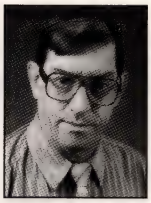
2. Grace, Roger, IEEE TC-9/NIST Smart-Transducer Interface Standard Information Gathering Project, May 1995.



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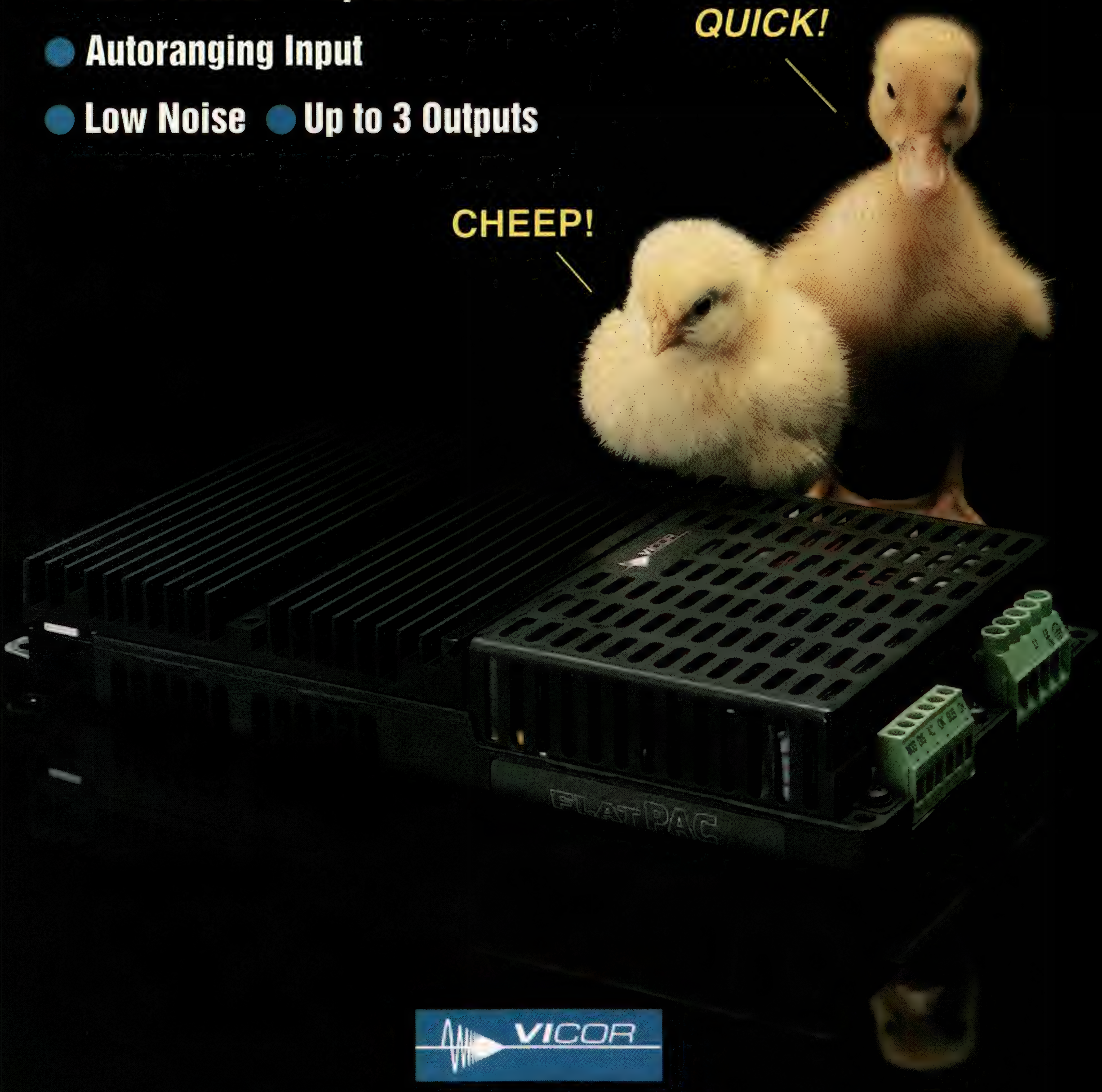

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CIRCLE NO. 125

YOU CAN HELP SET THE STANDARD

Before the workshop at the Sensors Expo (May 1995, Boston), the IEEE and NIST issued an information-gathering questionnaire to a select population. The form focused on the needs and desires of sensor designers. The IEEE and NIST also want your input. Your participation can enhance the statistical significance of the response by providing a larger population. Please check all responses that apply, and fax a copy to Roger Grace, at Roger Grace Associates: (415) 641-6156.

1. Respondent Information

a. Name ______________________________

c. Company ______________________________

d. Division ______________________________

e. Address ______________________________

b. Title ______________________________

f. Phone ______________________________

g. Fax ______________________________

h. E-mail ______________________________

2. What applications do you/your company address?

______ Automotive (1)
______ Medical (2)
______ Consumer (3)
______ Other (10)
______ Industrial controls (4)
______ Process control (5)
______ Factory automation (6)
______ Instrumentation (7)
______ Telecommunications (8)
______ Semiconductors (9)

3. What is/will be your company's primary involvement in smart-sensor or smart-actuator interfacing?

______ Sensor manufacturer (1)
______ Actuator manufacturer (2)
______ IC manufacturer (3)
______ Control-system manufacturer (4)
______ System integrator/VAR (5)
______ Specifying engineer (6)
______ End user (7)
______ Other (8)

4. What parameters do you need to measure, and in what format?

Parameter	**On/Off**	**Analog**	**Digital**
Pressure and derivatives	_____ (1a)	_____ (1b)	_____ (1c)
Acceleration and vibration	_____ (2a)	_____ (2b)	_____ (2c)
Flow	_____ (3a)	_____ (3b)	_____ (3c)
Level	_____ (4a)	_____ (4b)	_____ (4c)
Temperature	_____ (5a)	_____ (5b)	_____ (5c)
Position/proximity/presence	_____ (6a)	_____ (6b)	_____ (6c)
Chemical	_____ (7a)	_____ (7b)	_____ (7c)
Humidity/moisture	_____ (8a)	_____ (8b)	_____ (8c)
Mass	_____ (9a)	_____ (9b)	_____ (9c)
Force	_____ (10a)	_____ (10b)	_____ (10c)
Vision	_____ (11a)	_____ (11b)	_____ (11c)
Barcode	_____ (12a)	_____ (12b)	_____ (12c)
Other______________________	_____ (13a)	_____ (13b)	_____ (13c)

5. What output signal do your products currently offer, and what are your plans for the future?

Now	**In three years**	**Examples**
_____ (1a)	_____ (1b) Low-level output	0 to 50 mV
_____ (2a)	_____ (2b) Voltage, fixed	1 to 6V
_____ (3a)	_____ (3b) Voltage, ratiometric	0.5 to 4.5V; 5V supply
_____ (4a)	_____ (4b) Current	2-wire, 4 to 20 mA
_____ (5a)	_____ (5b) Frequency	1 to 10 kHz
_____ (6a)	_____ (6b) Pulse width	10 to 90%
_____ (7a)	_____ (7b) Digital	I^{2}C, Microwave, SPI
_____ (8a)	_____ (8b) Network	DeviceNet, LonWorks, SDS
_____ (9a)	_____ (9b) Other ______________________	

6. Which of the following functional features do you think are important to address in the proposed standard?

______ Redundancy (1)
______ Security (2)
______ Extensibility (3)
______ Network sense of time (4)
______ Support for the downloadable functionality (5)
______ Other (6) ______________________

7. Given that the proposed standard is to be an information model, which of the following functional features are important to you?

______ Uploading/downloading applications (1)
______ Security provisions (2)
______ Data in the model must be based on standard encoding (3)
______ Data in the model must be mapped onto existing data structure (4)
______ No opinion (5)

8. What portion of the information base must reside in the sensor?

List of object	______ Yes (1a)	______ No (1b)	______ No opinion (1c)
Object description	______ Yes (2a)	______ No (2b)	______ No opinion (2c)
Pointer-to-object description	______ Yes (3a)	______ No (3b)	______ No opinion (3c)
No preference	______		

9. Would you use an interface if defined at Level 1, 2, 3, or 4 (Fig 1)?

Level 1	______ Yes (1a)	______ No (1b)
Level 2	______ Yes (2a)	______ No (2b)
Level 3	______ Yes (3a)	______ No (3b)
Level 4	______ Yes (4a)	______ No (4b)

10. With reference to the definitions in Fig 1 for transducer, sensor/actuator, and networked smart sensor, what is your current and expected relative usage of these devices?

	Today	**In three years**
Transducer	______ % (1a)	______ % (1b)
Smart sensor/actuator	______ % (2a)	______ % (2b)
Networked smart sensor	______ % (3a)	______ % (3b)

11. What savings would you expect to realize as a result of implementation?

______ 0% (1)
______ 1 to 10% (2)
______ 10 to 25% (3)
______ 25 to 50% (4)
______ >50% (5)
____ Don't know (6)

12. What are the key benefits for systems and processes that you expect to achieve with the proposed standard? Check each in order of importance.

	Low	**Meduim**	**High**
Enhanced diagnostics	______	______	______
Ease of system design	______	______	______
Preventive maintenance	______	______	______
Reduced wiring installation costs	______	______	______
Ease of expandability/reconfiguration	______	______	______
Other	______	______	______

13. If you or your company has a plan for using or making communications networks at the sensor/actuator level, what are you working toward?

______ An open-system architecture (1)
______ A proprietary (closed) architecture (2)
______ No specific plan (3)

14. The proposed standard would operate over multiple underlying networks. List the one(s) you would prefer to see supported, in order of priority.

Priority 1 ____ (1)
Priority 2 ____ (2)
Priority 3 ____ (3)

15. Do you view the proposed development of this standard necessary in light of the activities of other standards committees, such as Fieldbus, IEC, ISA, and NEMA?

______ Yes (1) ______ No (2)

16. Do you agree with the general functional features/architectures proposed by the IEEE/NIST committee?

______ Yes (1) ______ No (2)

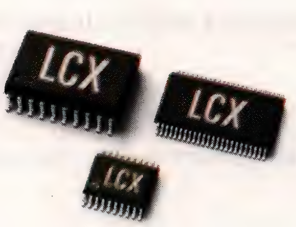
17. Would you personally serve on the standards committee?

______ Yes (1) ______ No (2)

18. May we contact you for further discussion?

______ Yes (1) ______ No (2)

INTRODUCING THE NEW STANDARD FOR LOW VOLTAGE LOGIC.



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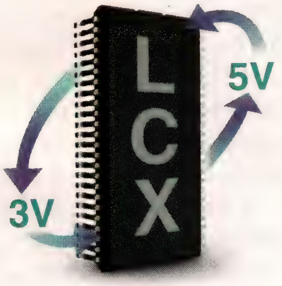

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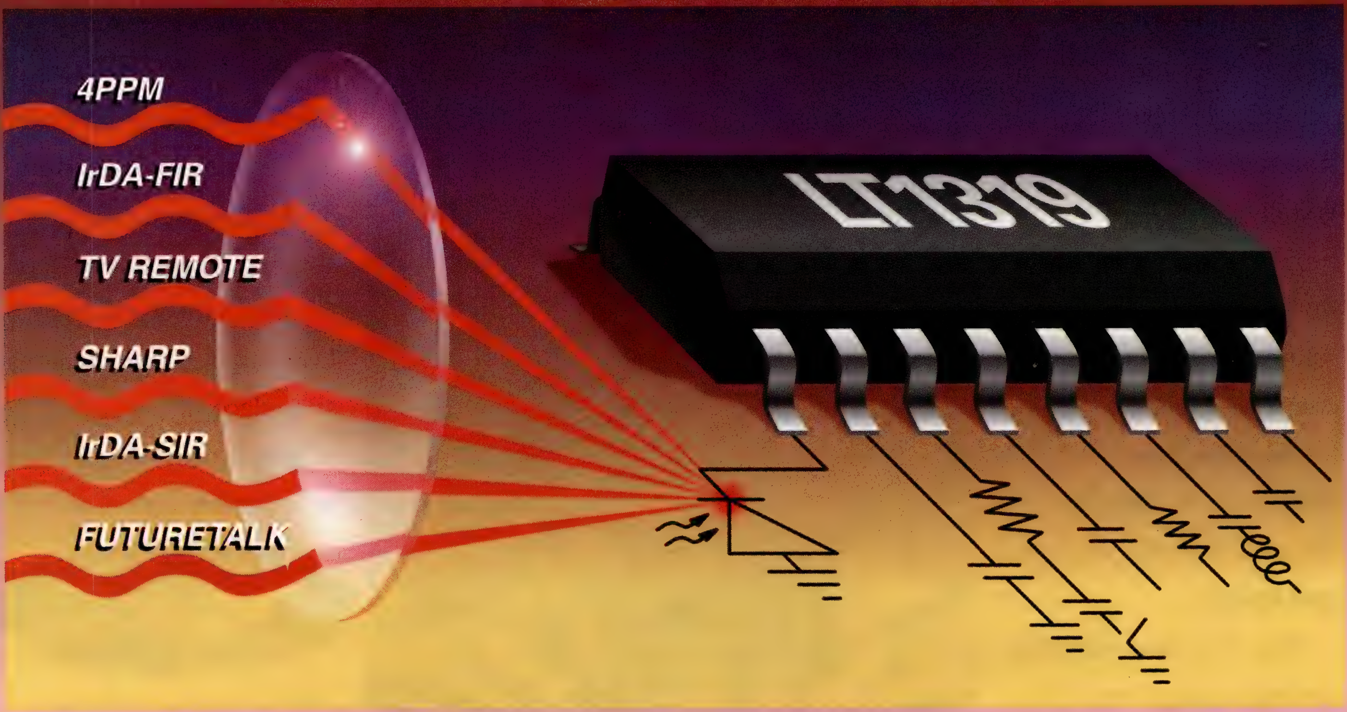
CIRCLE NO. 136

Multiple IR Standards, One Solution.



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Actual Size

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The LT1319 is a complete receiver with a photodiode preamplifier (15kΩ transimpedance), two gain channels and two on-board comparators (25ns and 60ns). It's flexible enough to handle data rates from TV remote and SIR all the way up to FIR and 4PPM (4MBaud). Optional external filtering permits rejection of high frequency fluorescents and reception of carrier-based protocols like Sharp/Newton ASK.

IR PROTOCOL	DATA RATE	SUPPORTED BY LT1319?
IrDA-SIR	115.2kBaud	YES
IrDA-FIR*	1.15MBaud	YES
IrDA-4PPM*	4MBaud	YES
SHARP/NEWTON	38.4kBaud	YES
APPLE MODULATED LOCALTALK	230kBaud	YES
TV REMOTE CONTROL	562 Baud	YES

**FIR and 4PPM are higher data rate extensions of IrDA-SIR.*

Input referred noise is a low 2pA/√Hz which provides high sensitivity and allows link lengths up to 2 meters. The 7MHz bandwidth supports data rates as high as 4MBaud. The LT1319 operates from a single 5V supply and in shutdown, supply current drops to 500µA.

The LT1319 comes in a narrow 16-pin surface-mount package. Pricing in 1000-piece quantities starts at $3.80.

For more details on **the** multi-protocol solution for IR applications, contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035. 408-432-1900. Fax: 408-434-0507. For literature only, call **1-800-4-LINEAR.**

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Programmable current source powers charger

CHESTER SIMPSON AND FRED HAMILTON, NATIONAL SEMICONDUCTOR, SANTA CLARA, CA

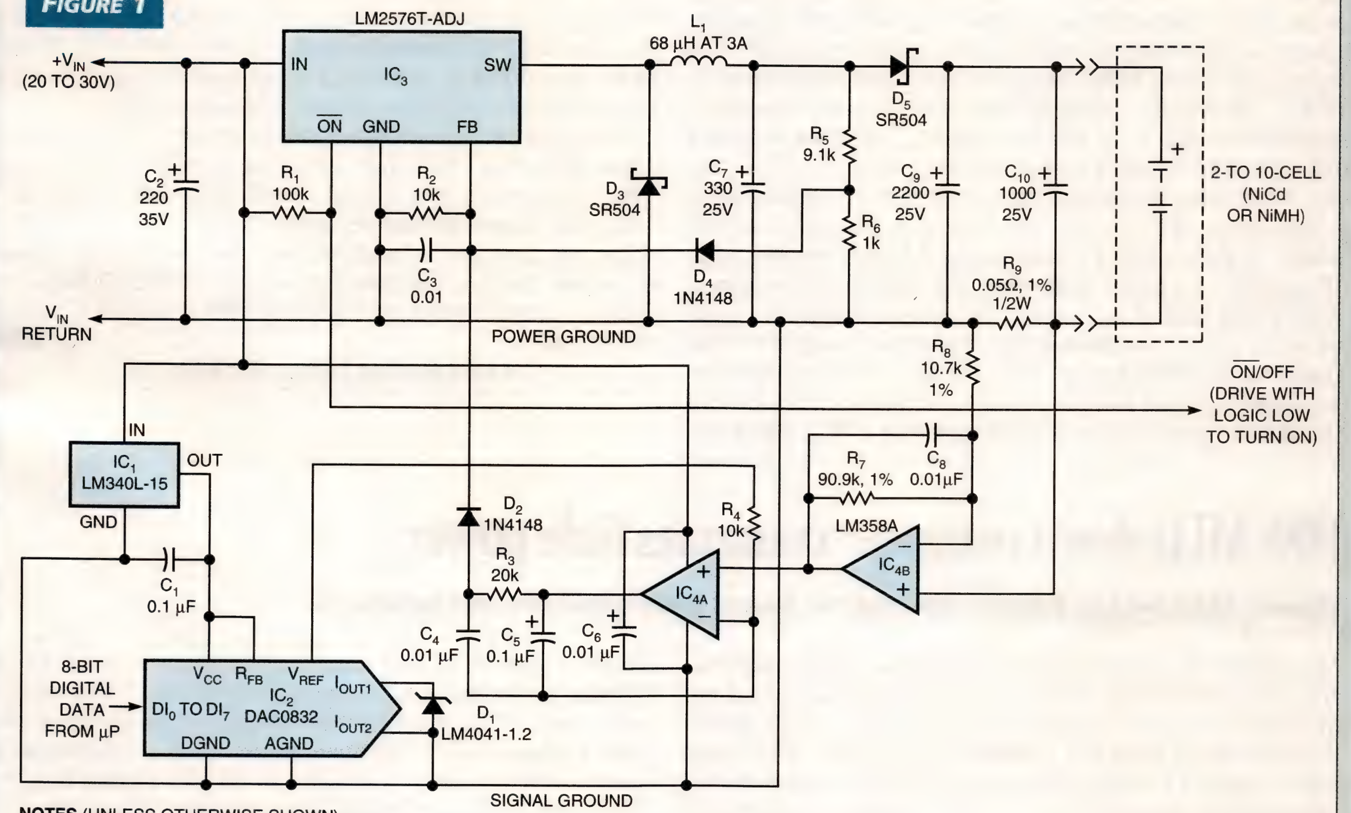
The circuit in **Fig 1** is a digitally programmable current source capable of sourcing currents as high as 2.55A. The circuit is intended for use in "smart chargers" (for NiCd or NiMH batteries containing as many as 10 cells) in applications that require fast recharge cycles. A smart charger contains a µP and sufficient memory to store exact charge/discharge profiles for different battery types and sizes. Many smart chargers "interrogate" a battery prior to charging and learn its specific needs from a ROM stored within the battery pack. The charger can thus safely charge different types of batteries from multiple manufacturers.

During the charge cycle, the charger constantly monitors the battery, compares its state with the optimum profile, and adjusts the charging current to hold it on target. This technique allows very fast charge cycles without harm to the battery—the battery never suffers from life-reducing overcharge. The fundamental building block for any smart charger is the current source used to charge the battery. The wish-list of features for this current source includes

- µP programmability
- good adjustment resolution with many available current levels
- high power-conversion efficiency to minimize charger heat dissipation
- wide input-voltage range, allowing use of an inexpensive, poorly regulated dc power source.

In **Fig 1**, the LM2576 step-down (buck) dc-dc converter serves as a current source to provide battery-charging current. The buck-regulator configuration provides good power-conversion efficiency. The charger operates as a constant-current source by sensing the voltage drop across R_9. The feedback loop holds this sense voltage constant. The DAC0832 D/A converter provides the dc voltage to the input of the error amplifier (IC_{4A}), which sets the voltage the feed-

FIGURE 1



NOTES (UNLESS OTHERWISE SHOWN):
1. ALL RESISTORS ARE 1/4W, 5%. ALL CAPACITORS ARE IN µF.
2. ALL CAPACITORS <1 µF ARE CERAMIC; ALL CAPACITORS >1 µF ARE ALUMINUM ELECTROLYTIC.
3. IC_3 REQUIRES SMALL HEAT SINK (THERMALLOY 7020 USED ON BREADBOARD).

This programmable current source, used in a "smart-charger" configuration, can charge batteries containing as many as 10 high-performance NiCd or NiMH cells.

back loop locks in, thus setting the charging current.

R_7 and R_8 set the gain of the sensing amplifier IC_{4B} such that a voltage of 0 to 1.22V from the output of the D/A converter produces a charging current of 0 to 2.55A in the battery. Because 255 programmed levels are available, the charging current can have any value from 0 to 2.55A in steps of 10 mA. (To obtain zero charging current, pull the ON pin of IC_3 high, possibly with an open-collector output.)

Detailed circuit operation

Buck-regulator IC_3 chops the input voltage at a switching frequency of 52 kHz and varies the pulse width as required by the load through the action of either the voltage- or current-control feedback loop. L_1, C_7, C_9, and C_{10} make up the output filter, which converts the square wave at the SW pin of IC_3 into a smooth dc voltage. Diode D_5 is a blocking diode that prevents the battery from discharging upon the removal of input power. Diode D_3 is the switching "catch" diode. Both diodes must be Schottky devices with at least 3A current rating.

R_9, IC_4, and associated components form the feedback loop that enables IC_3 to function as a constant current source. The role of IC_{4B} is to provide gain for the voltage developed across current-sense-resistor R_9 to correspond with the output of D/A-converter IC_2. Full-scale charging current (2.55A) must match the full-scale output of the D/A converter (1.22V) at the inputs of the current-error-amplifier IC_{4A}. In typical operation, the D/A converter presents a voltage through R_4 to the input of IC_{4A}, and the feedback loop fixes the charging current at the set value. C_8, C_5, C_4, R_3, and C_3 provide compensation for the current-control loop.

Although the charger operates as a constant current source in most cases, a voltage-control loop (comprising R_5, R_6, and D_4) is present to prevent the output of the charger from flying high if the battery disconnects from the charger. With the values shown, the maximum output voltage under no-load conditions is about 18.5V. The voltage-control (from D_4) and current-control (from D_2) signals are in a wired-OR connection at the feedback pin of IC_3. Either signal can thus control the pulse-width modulation of IC_3 as determined by the amount of load current.

With a battery connected to the charger output, the current-control loop supplies the feedback signal to IC_3 through diode D_2. However, upon battery disconnection, no charge current flows, and IC_{4A} holds its output low. This condition would cause IC_3 to go to maximum duty cycle (and hence maximum output voltage) if D_4 were not present.

The D/A-converter is configured in its "backwards" configuration, in which the R-2R resistor ladder operates in a voltage-dividing, rather than current-switching, mode. The output voltage at V_{REF} varies between 0 and 1.225V in 255 steps of 4.8 mV, corresponding to charging currents of 0 to 2.55A. IC_1 provides a constant 12V for IC_2. As IC_2 requires only a few milliamps to operate, the power dissipation in IC_1 and IC_2 is negligible.

Construction hints

Keep all leads and traces connected to the power ground (preferably a ground plane) as short as possible. Also, connect the ground lead of D_3 as close as possible to the ground connection of C_9. Tie the low-current signal-ground leads together, then connect them to power ground at a single point very near the ground connection of IC_3. Keep the leads of R_2 and C_3 as short as possible, and connect them very near the pins of IC_3. Connect the sense leads that drive IC_{4B} directly to the ends of R_9 to prevent errors from voltage drops in copper traces carrying the battery's return current.

Although the power-conversion efficiency of the circuit is high (84% with 25V input, 13V battery voltage, and 2.55A charging current), you'll need a small heat sink for IC_3. Any heat sink whose thermal resistance is ≤13°C/W is adequate, assuming a maximum ambient temperature of 60°C. Some examples include Thermalloy's 6032B, 7019B, 7020B, or 7021B; Aavid's 5903B or 5510B; or IERC's LATO127B4CB. (DI #1715) EDN

To Vote For This Design, Circle No. 390

900-MHz down converter consumes little power

RONALD MANCINI AND RAPHAEL MATARAZZO, HARRIS SEMICONDUCTOR, MELBOURNE, FL

Most 900-MHz down-converter designs are proprietary and, thus, are unavailable to the industry. The designs that are available are usually discrete or require high voltage, which excludes them from the portable market. The down converter in **Fig 1** is nonproprietary and suits battery-powered applications. Moreover, you can use the IC manufacturer's pc-board artwork to get a head start.

The heart of the down converter is a Gilbert cell, which consists of two long-tailed, differential-amplifier stages connected as two variable-transconductance amplifiers. Because the cell is constructed from the HFA3101 transistor array, the differential-amplifier stages are inherently matched. The inherent matching also reduces distortion resulting from thermal effects and mismatches in transistor beta and ohmic resistances. With the HFA3101 configured as shown, each pair of bases acts as a multiplier input. Thus, if you connect a local oscillator and an RF signal to the two inputs, the circuit generates the sum and difference frequencies. In this circuit, we select the difference frequency for the down conversion.

R_1, R_2, and R_3 form a voltage bias network to bias the long-tailed pairs; the circuit holds the bases of the current source, Q_5 and Q_6, at 1V and the bases of the inputs, Q_1 and Q_4, at 2.5V. Setting R_E at 27Ω yields emitter currents of approxi-

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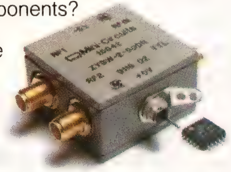

SPECIFICATIONS (typ)	Absorptive SPDT YSWA-2-50DR ZYSWA-2-50DR			Reflective SPDT YSW-2-50DR ZYSW-2-50DR		
Frequency (MHz)	dc-500	500-2000	2000-5000	dc-500	500-2000	2000-5000
Ins. Loss (dB)	1.1	1.4	1.9	0.9	1.3	1.4
Isolation (dB)	42	31	20	50	40	28
1dB Comp. (dBm)	18	20	22.5	20	20	24
RF Input (max dBm)	—	20	—	22	22	26
VSWR "on"	1.25	1.35	1.5	1.4	1.4	1.4
Video Bkthru (mV,p/p)	30	30	30	30	30	30
Sw. Spd. (nsec)	3	3	3	3	3	3
Price, $ (1-9 qty)	YSWA-2-50DR (pin) 23.95 ZYSWA-2-50DR (SMA) 69.95			YSW-2-50DR (pin) $14.95 ZYSW-2-50DR (SMA) 59.95		

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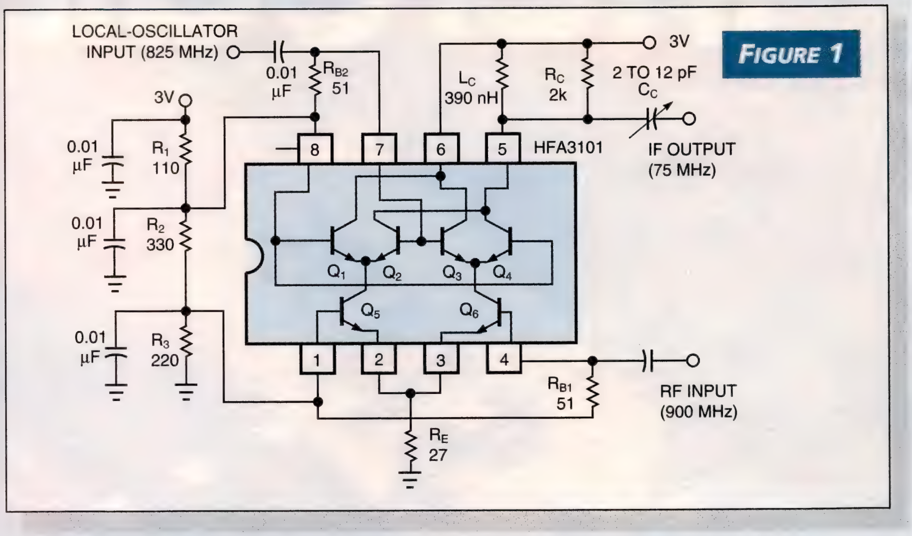
CIRCLE NO. 137

mately 5.5 mA, which is adequate to achieve the required bandwidth. This value of R_E is high enough so the quantity βR_E does not load the RF signal source. R_{B1} and R_{B2} terminate the transistor bases with 50Ω through the 0.01-μF decoupling capacitors, so the capacitors should be of high quality.

All the components should be leadless, with self-resonant frequencies exceeding 1 GHz. The output matching circuit comprising L_C, C_C, and R_C maximizes the gain. The selection of these components maximizes gain while allowing a 50Ω termination; the tuned, medium-Q matching network yields a 50Ω-to-2-kΩ transformation.

With the component values and frequencies in **Fig 1**, the circuit down converts 900 MHz to 75 MHz by using an 825-MHz local-oscillator signal, and it does so with 50Ω terminations. The circuit functions with supplies lower than 3V and draws comparatively low current for a down converter of this frequency. Thus, it's well-suited for battery-powered systems. You can obtain the pc-board artwork from the HFA3101 data sheet; you need no permission from Harris Semiconductor to use the pattern. (DI #1719)

FIGURE 1



This nonproprietary 900-MHz down converter is easy to configure and draws little power compared with circuits using discrete components.

To Vote For This Design, Circle No. 391

40V current source operates from –40 to +85°C

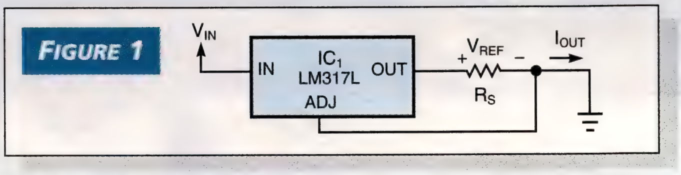
RAY SCOTT, SOR INC, LENEXA, KS

Wide-output-current-range sources that accommodate a wide supply and temperature range require special consideration. The basic circuit of (**Fig 1**) provides $I_{OUT} = V_{REF}/R_S$; typically, V_{REF} is 1.25V for the LM317L family. The LM317LZ is rated for 0 to +125°C; for lower temperature ranges, the LM317LBZ could be used (–40 to +150°C rating), but it is more costly and harder to obtain.

Fig 2's circuit uses commonly available components, including the LM317LZ, and can operate down to –40°C. It is designed for a current limit of 5 mA maximum. You select resistor R_1 to be ~10 times R_{SET}, making $I_{OUT}\approx 1.10\times I_{SET}$. (In reality, $I_{OUT}=I_{SET}+I_{R1}+I_{ADJ}$, so a better approximation is $I_{OUT}=1.15\times I_{SET}$). For I_{OUT} of 5mA, I_{SET} is 4.5 mA. R_{SET} is V_{REF}/I_{SET}, so 1.25V/4.35mA=287Ω, and $R_1=10\times R_{SET}$=2.87 kΩ. In this case, R_1 and R_{SET} are standard 1% values and I_{OUT} does equal 5 mA. In cases that are not exact, select R_1 as close to the calculated value as possible and vary it to trim in the correct value of I_{OUT}. (Don't stray too far from the 10:1 ratio of R_1 to R_{SET}, though.)

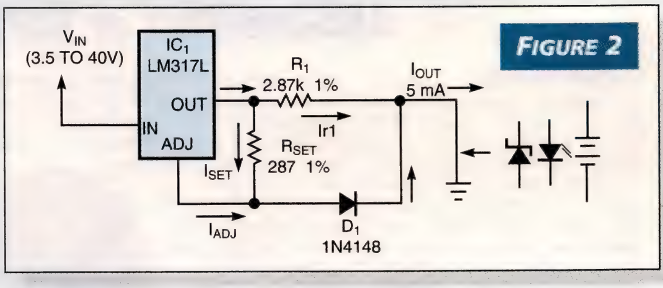
The temperature coefficient of D_1 offsets that of the LM317LZ, so a temperature range of –40 to +85°C will alter the current limit less than ±100 μA for the 5-mA limit shown. This works for currents from 2.5 to over 20 mA with no special heatsinking and accommodates V_{IN}–V_{OUT} of 40V dc. To use the current source/limit, place an LED, zener diode, switch, etc. in series with the circuit as shown. V_{IN} minimum should be 3.5V plus the voltage drop of the series device. Resistors of 1% tolerance were used for initial accuracy and repeatability, but you could use 5% values for reduced cost. (DI #1721)

FIGURE 1



The basic circuit above provides regulated output current but will not work down to –40°C because of component limitations.

FIGURE 2



This circuit overcomes the limits in Fig 1 with low-cost components.

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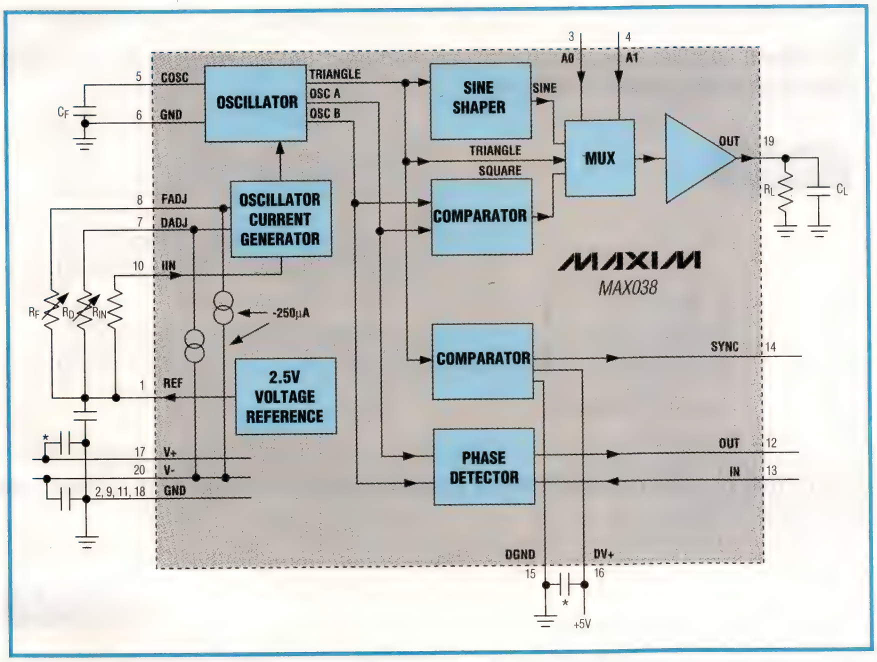

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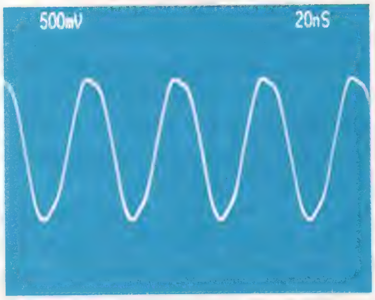
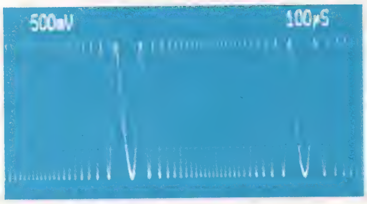
SINE-WAVE OUTPUT (20MHz)



FREQUENCY MODULATION



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CIRCLE NO. 138

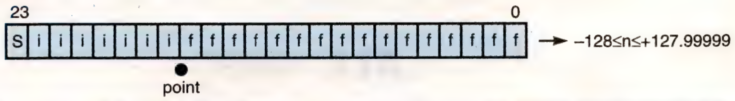
Hardware add-on provides mixed-format multiply

Patrice Nus and Vladimir Bochev, Université Henri Poincare de Nancy, Saint Die, France

Fixed-point-DSP users are aware of overflow problems that frequently occur in current algorithms such as digital filtering. Many solutions to problems such as floating point or block floating point exist; these methods, however, are cumbersome and slow to execute on fixed-point machines. An alternative is to adopt a mixed-number format consisting of an integer and a fractional part. This technique is particularly attractive for fixed-point processors with wide data words expressed in bits. An example is the 24-bit DSP56001 from Motorola. **Fig 1** shows a possible fit and the covered range for such a format.

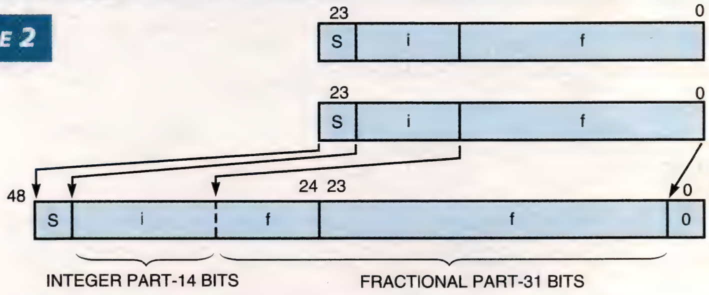
This representation—with one sign bit, seven bits for the integer part, and 16 bits for the fractional portion—particularly suits DSP algorithms (and receives implicit support from Motorola). Its advantage is straightforward use of the DSP's multiplier. However, the

FIGURE 1



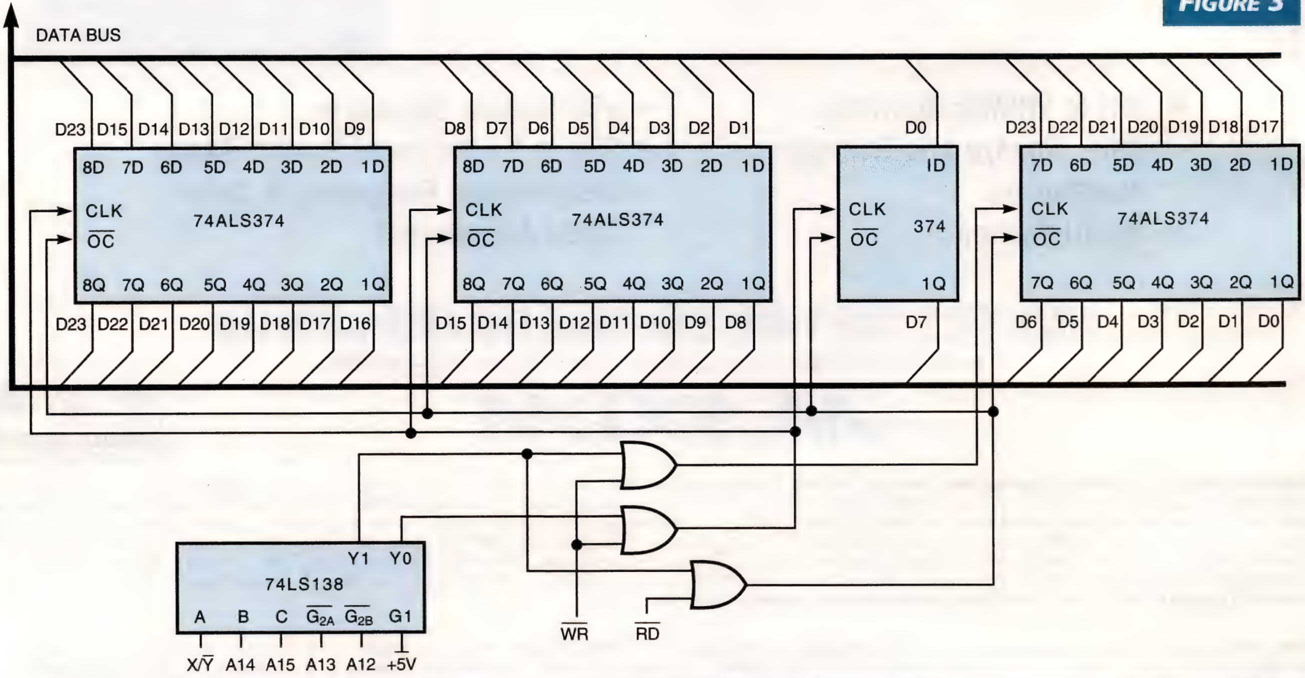
This mixed-number format, with integer and fractional parts, suits fixed-point DSP chips such as Motorola's DSP56001.

FIGURE 2



This format results from performing a multiply using mixed-format numbers such as the one in Fig 1.

FIGURE 3



This simple hardware aid speeds mixed-format multiplication using the DSP560001.

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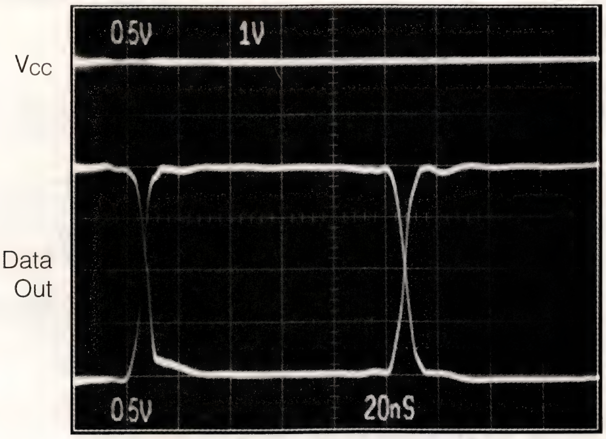
10Mbps at 3.0V Into 54Ω Load!



The MAX3485 runs at 10Mbps into 54Ω, easily meeting the 1.5V output specification.

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MAX3483	0.25	3.0 to 3.6	Half	Yes	Yes	2	75176
MAX3485	10		Half	No	Yes	2	75176
MAX3486	2.5		Half	Yes	Yes	2	75176
MAX3488	0.25		Full	Yes	No	—	75179
MAX3490	10		Full	No	No	—	75179
MAX3491	10		Full	No	Yes	2	75180

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CIRCLE NO. 139

format of the result is unsuitable for further computations (**Fig 2**).

It's necessary to reformat, but, unlike Analog Devices' ADSP210x or Texas Instruments' DSPs, the DSP56001 doesn't come equipped with a barrel shifter. So, the DSP56001 must execute the program fragment in **Listing 1** to reformat. The whole process takes 10 cycles, which isn't negligible in a lengthy loop. The simple hardware fix in **Fig 3** speeds this computing situation. After a mixed-format multiplication, you should save the result in a register, from which you can read it suitably reformatted. The program fragment in **Listing 2** performs the reformatting in just four cycles.

LISTING 1—DSP CODE FOR REFORMATTING NUMBERS WITH FIG 2 FORMAT

```
                                                            Prog   Icyc
                                                            word
mpy    x0,x1,a      ; x0.x1 → a                               1      1
rep    #7           ; repeat 7 times the "asl a" instruction  1      2
asl    a            ; arithmetically shift a one bit to the left  1  7
```

LISTING 2—DSP CODE FOR REFORMATTING WITH FIG 3 HARDWARE AID

```
                                                               Prog   Icyc
                                                               word
mpy    x0,x1,a      ; x0.x1  → a                                 1      1
move   a,l:(R0)     ; save a, address register R0 contains $800  1      2
move   x:(R0),a     ; read the mixed format result               1      1
```

The circuit count is six IC packages. Because it's essentially a bus circuit, you can implement it as an add-on in existing systems (provided the system is designed to accept extensions). Alternatively, you could configure the circuit using about one-third of a single Xilinx FPGA 2000 or 3000 Series. Using the FPGA, the circuit count is two, because of the required eight-pin Xilinx serial initialization PROM (or some other popular PROM like the 27xxx Series). (DI #1713) EDN

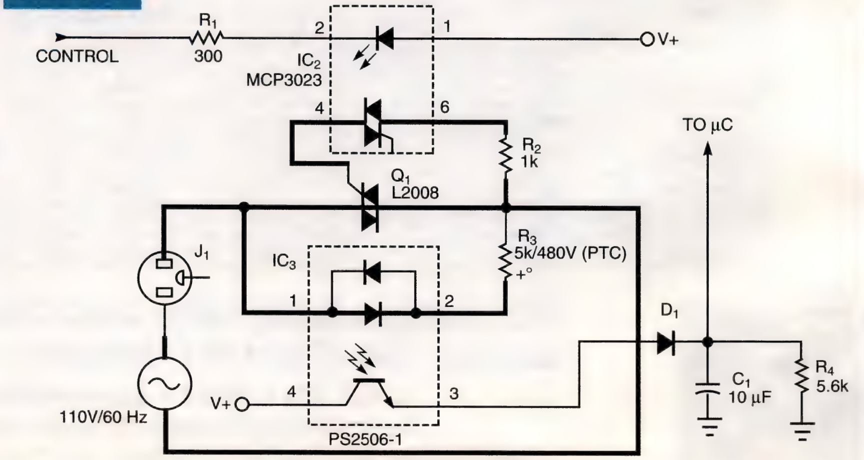
To Vote For This Design, Circle No. 393

Microcontroller watches, controls ac power

SAMUEL KEREM, INFRARED FIBER SYSTEMS, SILVER SPRING, MD

For monitoring and controlling a power circuit from a microcontroller (µC), **Fig 1** replaces the conventional technique of a low-value resistor and differential amplifier (with gain set for the expected current value). A control line turns triac Q_1 on and off via optoisolator IC_2. When an appliance is plugged into J_1 and turned on, the voltage drop across Q_1 is independent of the current value and sufficient to turn on optoisolator IC_3. The phototransistor current of IC_3 charges C_1 to a logic 1, which is sensed by the µC. When IC_2 is on, but the device in J_1 is actually turned off (by its own switch), there is no current through Q_1, and the sense line is at logic 0 because C_1 is discharged through R_4.

FIGURE 1



This circuit allows an isolated microcontroller to both sense and control ac power to an externally plugged-in device. The lines in boldface in the schematic are electrically isolated from the signal lines.

When the µC turns Q_1 off (even though the device in J_1 is still switched on and therefore conducting), current flows through pins 1 and 2 of IC_3, as well as R_3 (a positive-temperature-coefficient resistor with a large resistance change resulting from a small temperature change). In this case, R_3 sharply increases its resistance to keep the current flowing through it at about 15 to 20 mA. However, even though C_1 is charging to logic 1, the µC "knows" the device is not really on, because it has set power switch Q_1 to the off state via the control line. (DI #1722) EDN

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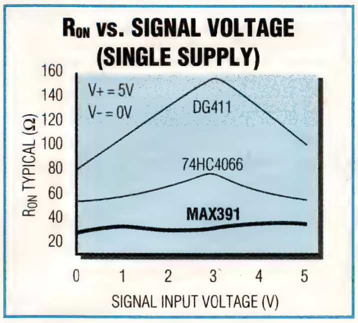
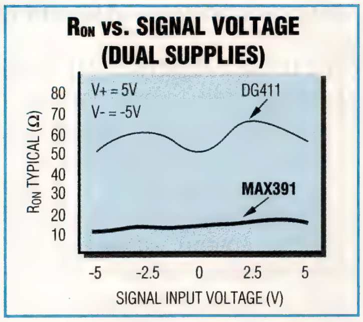


The MAX391's flat on-resistance prevents signal errors in high-resolution data-acquisition systems.

Don't sacrifice performance in your low-voltage system by using retested and respecified analog switches and muxes that were designed for high-voltage applications. Maxim's **all new** family of analog switches and muxes is designed to give the maximum performance at single-supply operation of +2.7V to +16V and dual supplies of ±2.7V to ±8V. These new devices are pin-compatible with many high-voltage, industry-standard parts, and the MAX320–MAX325 come in space-saving, 8-pin µMAX packages.

ACTUAL SIZE



Prevent harmonic distortion in audio systems with the MAX391's flat on-resistance.

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DEVICE	FUNCTION	ON-RESISTANCE MATCH (Ω max)	ON-RESISTANCE FLATNESS (Ω max)	CHARGE INJECTION (pC max)	PIN COMPATIBLE	µMAX PACKAGE
SWITCHES						
MAX320	Dual SPST (NO)	2	6	5		✔
MAX321	Dual SPST (NC)	2	6	5		✔
MAX322	Dual SPST (NO, NC)	2	6	5		✔
MAX323	Dual SPST (NO)	2	6	5		✔
MAX324	Dual SPST (NC)	2	6	5		✔
MAX325	Dual SPST (NO, NC)	2	6	5		✔
MAX381	Dual SPST (NO)	2	6	5	DG401	
MAX383	Dual SPDT	2	6	5	DG403	
MAX385	Dual DPST (NO)	2	6	5	DG405	
MAX391	Quad SPST (NC)	2	6	5	DG411	
MAX392	Quad SPST (NO)	2	6	5	DG412	
MAX393	Quad SPST (NO, NC)	2	6	5	DG413	
MAX394	Quad SPST	2	6	5	MAX333	
DEVICE	**FUNCTION**	**ON-RESISTANCE MATCH (Ω max)**	**ON-RESISTANCE FLATNESS (Ω max)**	**CHARGE INJECTION (pC max)**	**PIN COMPATIBLE**	**LATCHED INPUT**
MUXES						
MAX382	8-Channel Mux	10	16	5	DG428	✔
MAX384	Dual 4-Channel Mux	10	16	5	DG429	✔
MAX395**	8-Channel Mux	10	16	5	MAX335	SERIAL CONTROL
MAX396*	16-Channel Mux	10	16	5	DG406	
MAX397*	Dual 8-Channel Mux	10	16	5	DG407	
MAX398	8-Channel Mux	10	16	5	DG408	
MAX399	Dual 4-Channel Mux	10	16	5	DG409	

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* Available June 1995.
** Available after August 1995.

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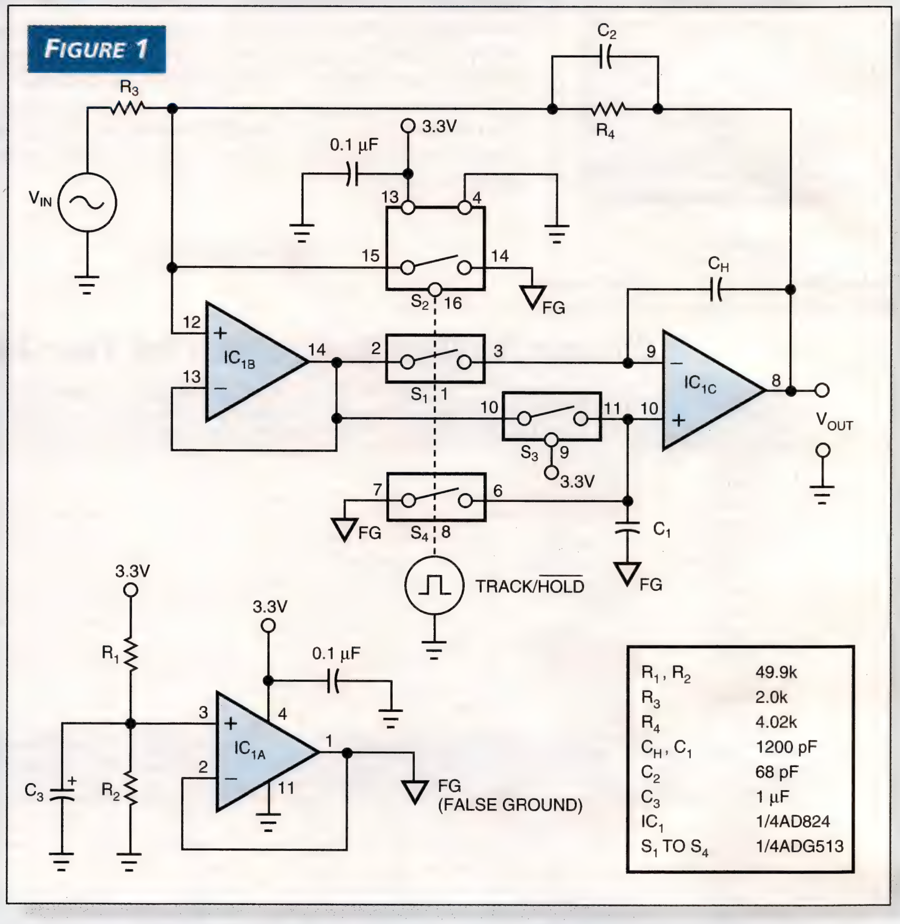
Precision T/H amplifier uses 3.3V supply

JOHN MCDONALD, ANALOG DEVICES, SANTA CLARA, CA

FIGURE 1



R$_1$, R$_2$	49.9k
R$_3$	2.0k
R$_4$	4.02k
C$_H$, C$_1$	1200 pF
C$_2$	68 pF
C$_3$	1 μF
IC$_1$	1/4AD824
S$_1$ TO S$_4$	1/4ADG513

This track-and-hold amplifier operates from a 3.3V supply. It has compensation circuitry to minimize both track-to-hold pedestal and feedthrough.

The track-and-hold (T/H) circuit in **Fig 1** works well in applications using a low-voltage single supply, such as in battery-powered designs. Despite the low supply voltage, output-signal dynamic range remains high thanks to the rail-to-rail output swing of the amplifiers and switches. S/N ratio is also high because of the wide output-signal range and low amplifier noise. By using a quad JFET op amp and a quad analog switch, the T/H circuit also features low parts count (12 parts total) and small board real estate (with SOICs, $<\frac{3}{4}$ in.^{2}). Circuit parameters include acquisition time of less than 4.5 μsec (1V step to 1%), settling time of less than 300 nsec to 1%, and a track-mode bandwidth of 40 kHz.

During track mode, S$_1$ and S$_4$ are closed, and S$_2$ is open. The circuit transfer function is thus $V_{OUT}=-2V_{IN}$. S$_1$ and S$_4$ open, and S$_2$ closes for hold mode. The hold-mode output remains constant at the output voltage that immediately preceded the hold command. During the transition from track to hold mode, S$_4$ reduces the pedestal, or hold-step, error by injecting the same amount of charge (typically 11 pC) into the noninverting input of IC$_{1C}$ that S$_1$ injects into the inverting input. This equal injection creates a common-mode voltage that IC$_{1C}$ rejects by the amount of its CMRR. Pedestal error for this circuit is less than 3 mV over the entire 0 to 3.3V input range. Increasing C$_H$ and C$_1$ reduces pedestal error further—but at the expense of increased acquisition time.

As a result of S$_1$ feedthrough, an attenuated and undesired input signal appears at the inverted input of IC$_{1C}$ during hold mode. S$_3$ remains open in both modes and allows feedthrough of the input signal to the noninverting input of IC$_{1C}$. Because S$_1$ and S$_3$ exhibit similar feedthrough characteristics, the common-mode rejection of IC$_{1C}$ reduces signal feedthrough by more than 60 dB. Inverting-amplifier configurations in single-supply applications require a false-ground reference. In this circuit, R$_1$ and R$_2$ divide the supply voltage symmetrically, and IC$_{1A}$ buffers the voltage and thus creates a low-impedance false-ground reference for the T/H circuit.

Hold-mode droop rate is proportional to parasitic current. Quad JFET op amps are well-suited for T/H circuits because of their low input-bias-current specifications (typically 3 pA for the AD824). By using JFET op amps and low-leakage (<100 pA) CMOS switches, this design keeps droop lower than 20 mV/sec. Higher values of C$_H$ produce lower droop rates. C$_H$ and C$_1$ should be polystyrene, polypropylene, or Teflon capacitors, because these types exhibit low leakage and dielectric absorption. The design uses metal-film resistors of 1% tolerance. Finally, using the ADG513 CMOS switch simplifies the switch-control circuitry to only one line, because this device has two normally open and two normally closed switches. (DI #1717) EDN

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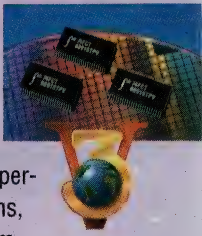

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Signal chopping enhances bridge performance

JEROME JOHNSTON, CRYSTAL SEMICONDUCTOR, AUSTIN, TX

You can implement signal-chopping techniques, such as those found in CMOS chopper-stabilized amplifiers, at the system level to obtain the offset stability of chopper amplifiers. Moreover, you'll obtain the better noise performance of bipolar amplifiers. The bridge measurement system in **Fig 1** uses the MIC4428 driver to "chop" the bridge excitation, with polarity reversal upon command from the system microcontroller (μC). The DG303 multiplexer selects either the bridge output or a voltage proportional to the bridge excitation.

The A/D converter (operating in bipolar mode) yields a conversion word for each phase of the two phases of the excitation: one positive and one negative. The negative conversion word then subtracts from the positive conversion word to yield a result that's free from system offsets. The μC computes offset-corrected samples for each of the multiplexer signals: the bridge output and bridge excitation. The μC then takes the ratio of these two to compute the final output conversion word, which is free of any drift in the excitation supply.

Each time the bridge excitation or the multiplexer switches, allow time for the amplifier to settle before the 20-bit CS5504 A/D converter starts a new conversion. The converter can operate at speeds as high as 100 samples/sec. The system achieves an offset drift lower than 100 nV p-p over slowly varying temperature conditions, and it yields more than 100,000 noise-free counts at two updates/sec after averaging five conversion words. Channel 2 of the A/D converter serves to monitor the temperature of the load cell, whose temperature profile you can record during system calibration. (DI #1720) EDN

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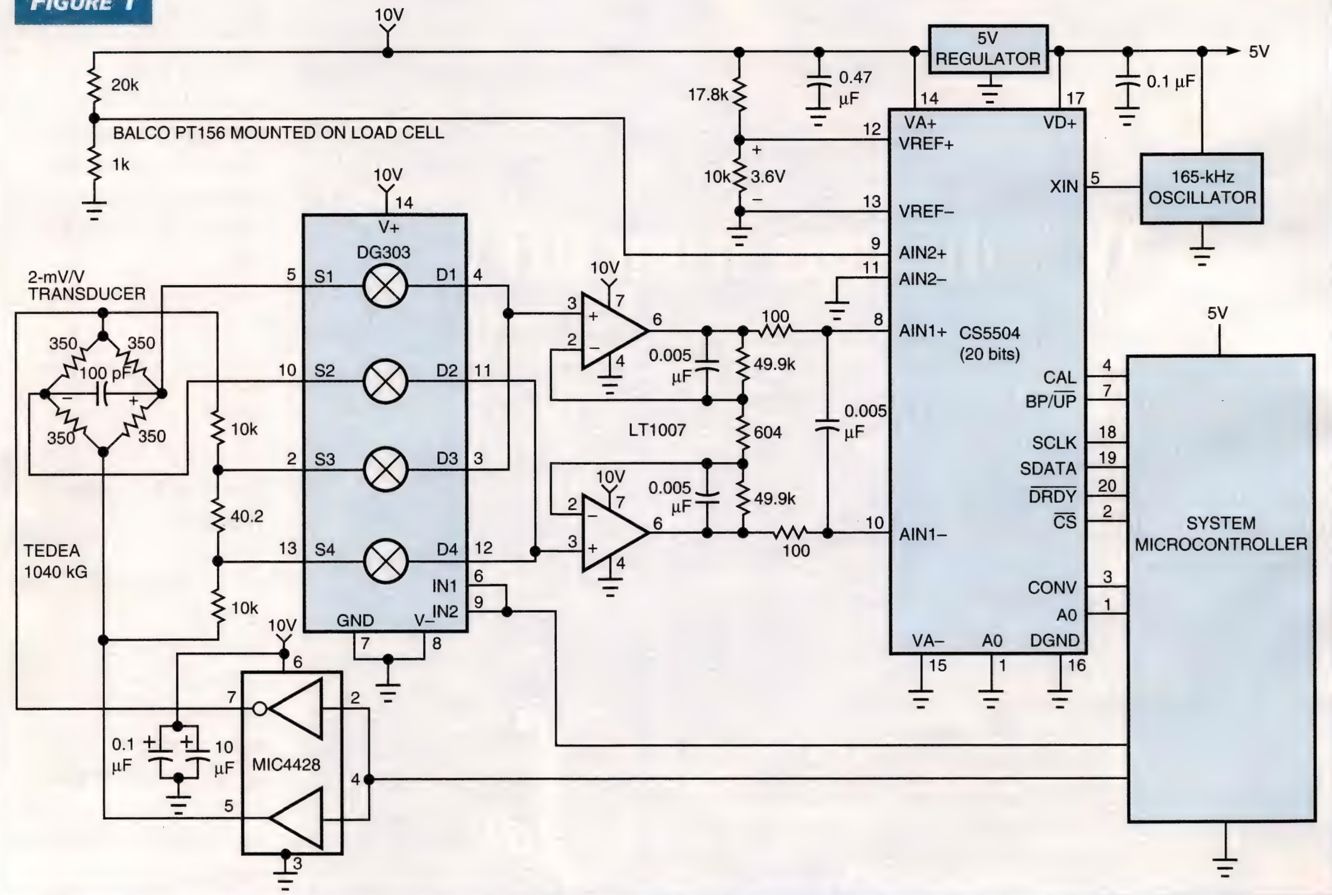
FIGURE 1



This bridge measurement system yields the offset stability of chopper-stabilized CMOS amplifiers—but with the superior noise performance of bipolar amplifiers.

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Counter IC provides wait states for 8031/8051

Y S TAM, CANADIAN MARCONI CO, OTTAWA, ON, CANADA

When you connect a slow device to a µC, you insert a number of wait states to extend the read or write cycle. For the 8031 or 8051 family, however, no input is available for extending the cycle. So, to extend the cycle, stretch the period of the clock connected to the µC's XTAL1 input. In **Fig 1**, IC$_3$ is an up/down counter configured as a down counter, with the number of wait states preset at inputs A to D. The preset IC$_4$ enables the clock connected to the µC's XTAL1 input.

When you address IC$_1$ with a low state on either CPU_RD or CPU_WR, pin 3 of IC$_2$ switches high and allows IC$_3$ to start counting down. Pin 6 of IC$_4$ goes high to stretch the clock period. When counter IC$_3$ reaches zero, pin 12 of IC$_3$ goes high and stops the counting. Pin 6 of IC$_4$ switches from high to low at the next low-to-high transition of the clock, thereby reenabling the clock. Certain 8031 or 8051 family members have a minimum requirement on the clock frequency which is not so for the 80CL31 and 80CL51 from Philips. (DI #1718) EDN

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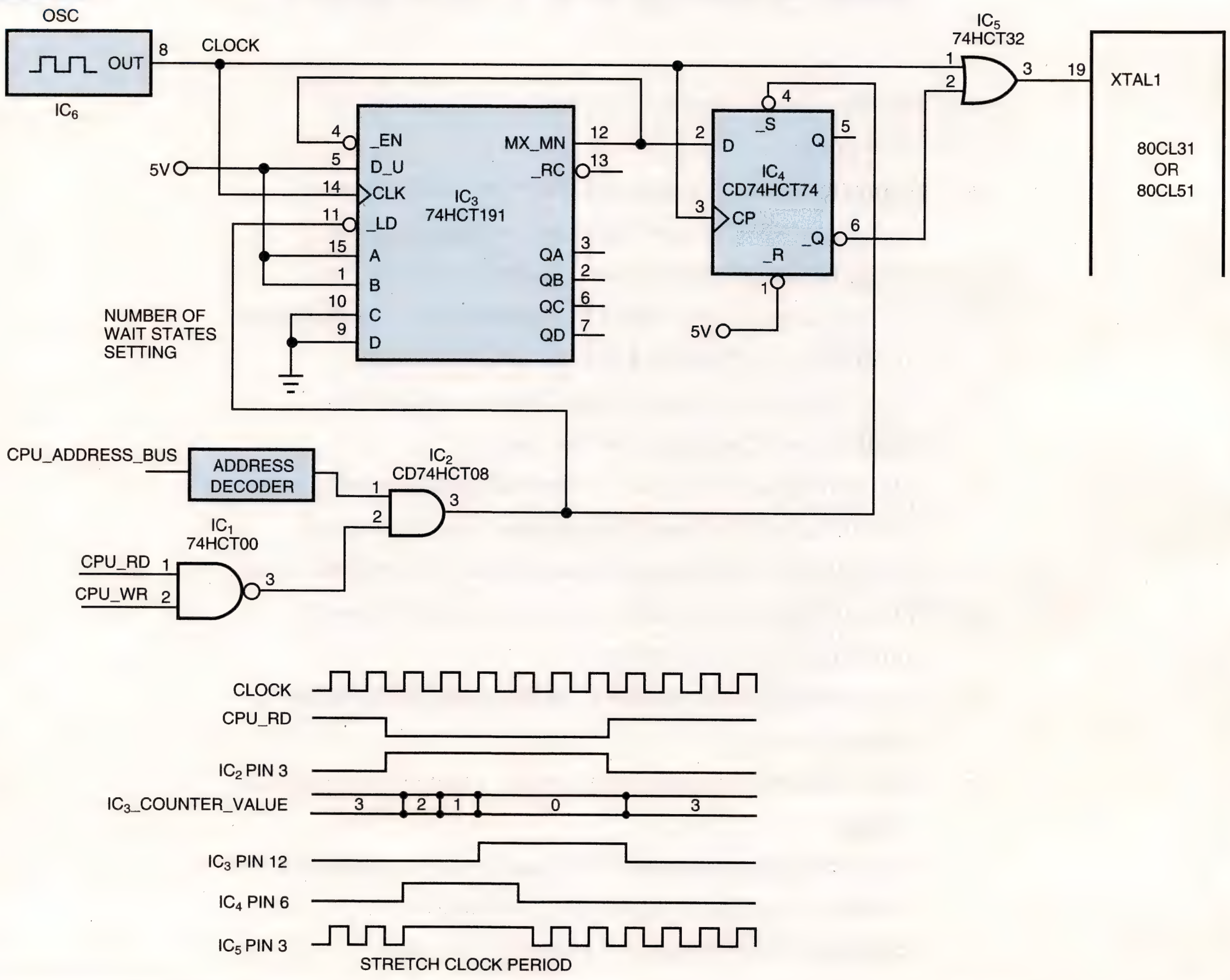
FIGURE 1



Use an up/down counter to configure a wait-state generator for the 8031 or 8051 µC, which offers no input for extending read or write cycles.

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The winning Design Idea for the November 10, 1994, issue is entitled "Oscillator keeps THD below 1 ppm," submitted by Jeff Smith of Analog Devices (Wilmington, MA).

LINEAR TECHNOLOGY

DESIGN NOTES

The LTC1392: Temperature and Voltage Measurement in a Single Chip – Design Note 106

Ricky Chow and Dave Dwelley

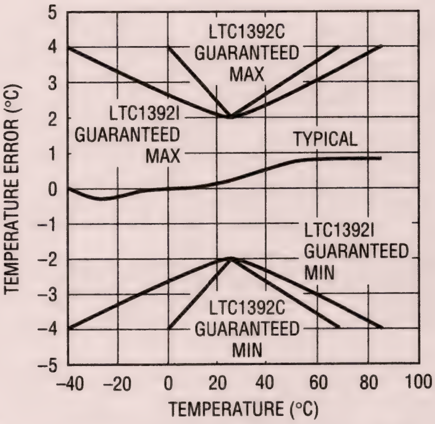
Introduction

The LTC®1392 is a new micropower, multifunction data acquisition system designed to measure ambient temperature, system power supply voltage and power supply current or differential input voltage. No external components are required for temperature or voltage measurements, and current measurements can be made with a single low value external resistor. An on-board 10-bit A/D converter provides a digital output through a 3- or 4-wire serial interface. Supply current is only 350μA when performing a measurement; this automatically drops to less than 1μA when the chip is not converting. The LTC1392 is designed to be used for PC board temperature and supply voltage/current monitoring or as a remote temperature and voltage sensor for monitoring almost any kind of system. It is available in SO-8 and DIP packages allowing it to fit onto almost any circuit board.

Measurement Performance

Wafer level trimming allows the LTC1392 to achieve guaranteed accuracy of ±2°C at room temperature and ±4°C over the entire operating temperature range. The 10-bit A/D converter gives 0.25° resolution over the 0°C to 70°C (LTC1392C) or −40°C to 85°C (LTC1392I) range. Temperature is output as (ADC code/4) − 130°C with a theoretical maximum range of −130°C to 125.75°C. Figure 1 shows the typical output temperature error of the LTC1392 over temperature.

In supply voltage monitor mode, the A/D converter makes a differential measurement between the 2.42V reference and the actual power supply voltage. Each LSB step is equal to approximately 4.727mV, giving a theoretical measurement range of 2.42V to 7.2V. The LTC1392 has guaranteed accuracy over a voltage range of 4.5V to 6V, with a total absolute error of ±25mV or ±40mV respectively, over the commercial or industrial temperature range.



DN106 • F01

Figure 1. Output Temperature Error

Voltage is output as (ADC code × 4.727mV) + 2.42V. Figure 2 shows typical integral and differential nonlinearity performance of V_{CC} measurement.

The differential voltage input mode can be configured to operate in either 1V or 0.5V unipolar full-scale mode. Each mode converts the differential voltage between input pins V^+ and V^- directly to bits with the output code equal to ADC code × (full scale/1024). The 1V mode is specified at 8 bits accuracy with the eighth bit accurate to ±0.5LSB or ±2mV, while the 0.5V full-scale mode is specified to seven bits accuracy ±0.5LSB, giving the same ±2mV accuracy. The differential inputs include a common-mode input range including both power supply rails allowing them to be used to measure the voltage across a sensor resistor in either leg of the power supply. They can also be used to make a unipolar differential transducer bridge measurement or to make a single-ended voltage measurement by grounding the V^- pin.

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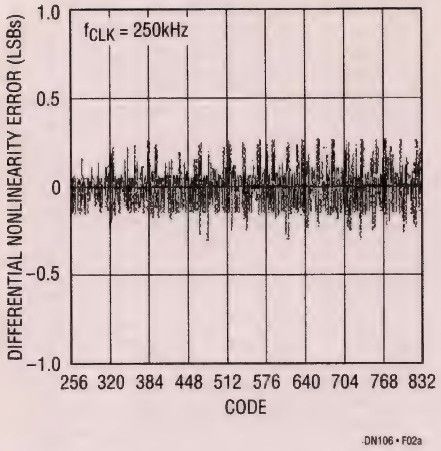

Figure 2a. Differential Nonlinearity, Power Supply Voltage Mode

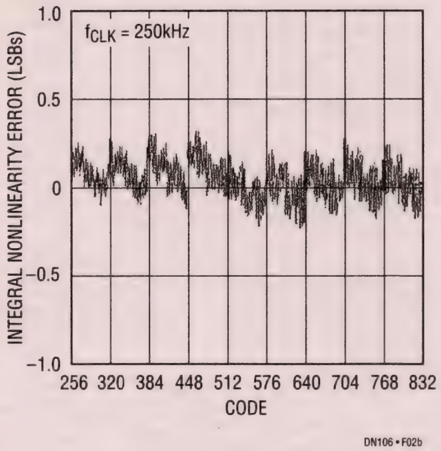

Figure 2b. Integral Nonlinearity, Power Supply Voltage Mode

The serial interface in the LTC1392 allows all of its functionality to be implemented in an 8-pin SO or DIP package and makes connection easy to virtually any MPU. Four pins are dedicated to the serial interface: active low chip select ($\overline{CS}$), clock (CLK), data input (D_{IN}) and data output (D_{OUT}). The D_{IN} pin is used to configure the LTC1392 for the next measurement and the D_{OUT} pin outputs the A/D conversion data. The D_{IN} pin is disabled after a valid configuration word is received and the D_{OUT} pin is in three-state mode until a valid configuration word is recognized, allowing the two pins to be tied together in a 3-wire system. The serial link allows several devices to be attached to a common serial bus, with separate $\overline{CS}$ lines to select the active chip.

Typical Application

A typical LTC1392 application is shown in Figure 3. A single point "star" ground is used along with a ground plane to minimize errors in the voltage measurements. The power supply is bypassed directly to the ground plane with a 1μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor.

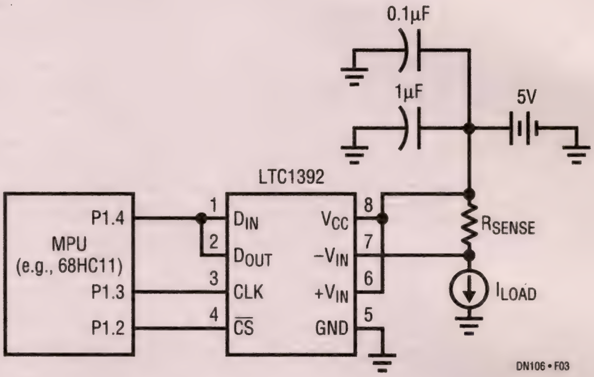

Figure 3. Typical Application

Conclusion

The LTC1392 provides a versatile data acquisition and environmental monitoring system with an easy-to-use interface. Its low supply current, coupled with space-saving SO-8 or DIP packaging make the LTC1392 ideal for systems which require temperature, voltage and current measurement while minimizing space, power consumption and external component count. The combination of temperature and voltage measuring capability on one chip make the LTC1392 unique in the market providing the smallest, lowest power multifunction data acquisition system available.

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Self-calibrating ADCs offer accuracy, flexibility

SEAN O'LEARY, ANALOG DEVICES INC

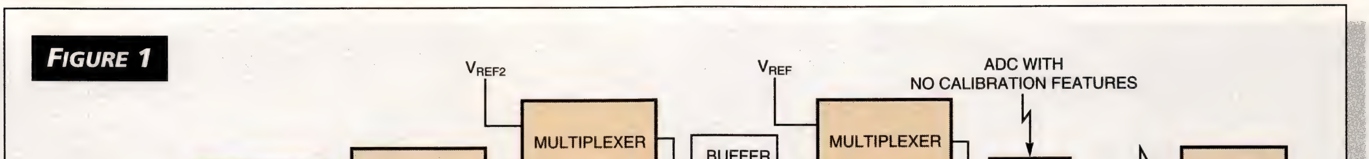
Using converters with built-in calibration eases design of an analog signal chain with greater accuracy and fewer calibration-related components. This calibration affects what you can achieve in accuracy and linearity and the hardware and software effort required.

An important issue in A/D design is how to achieve system accuracy. You need to look at minimizing errors in the analog signal path from its source through the ADC. System-offset and system-gain errors describe path errors, and ADC-offset, converter-gain, and converter-linearity errors describe errors within the ADC.

An ADC with built-in calibration features simplifies your circuitry and eases your ability to correct system-offset and system-gain errors (**Fig 1**). Converters with such calibration provide cost and performance advantages over conventional ADCs. An RC network on the analog input pins that filters out noise may introduce a gain error on the analog input voltage. However, system calibration can remove this gain error.

ADCs with calibration capability offer advantages that go beyond performance and the system-design implications. The vendor can achieve a lower cost design and fabrication

FIGURE 1

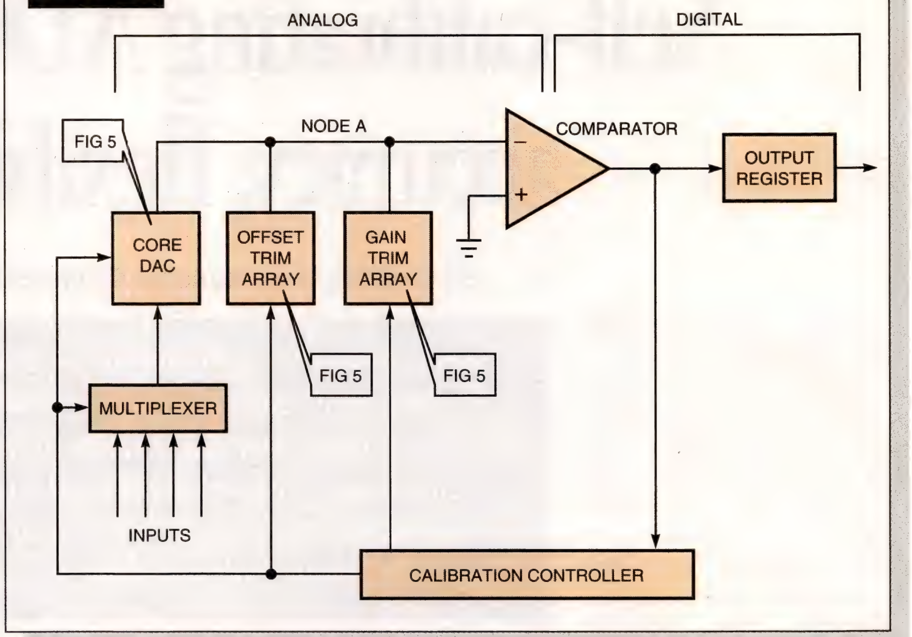


This analog signal path uses an ADC with and without self-calibration features ((b) and (a), respectively). In (a), the processor controls various trim inputs to the scaling and gain amplifiers and as multiplexers, switching in inputs to compensate for errors.

process in which calibration, rather than inherent design, removes the errors. This capability reduces the cost of the device for the user, shortens the converter's design cycle, and provides a wider selection of converters for the design window.

You can program the ADC to the analog input range in your system entirely in software, which saves components and space. Therefore, you do not have to worry about having your analog input range correspond to the voltage the converter data sheet specifies. You do not have to calculate the drift of critical parameters and specifications over temperature. Many data-sheet specifications are normally given only at nominal temperature, such as 25°C, along with a TC-drift value. Instead of spending time calculating error budgets and performance at the temperature extreme, the calibrating converter automatically adjusts to the new temperature without needing calculations.

FIGURE 2



A sampling ADC shows calibration-related functions and a controller.

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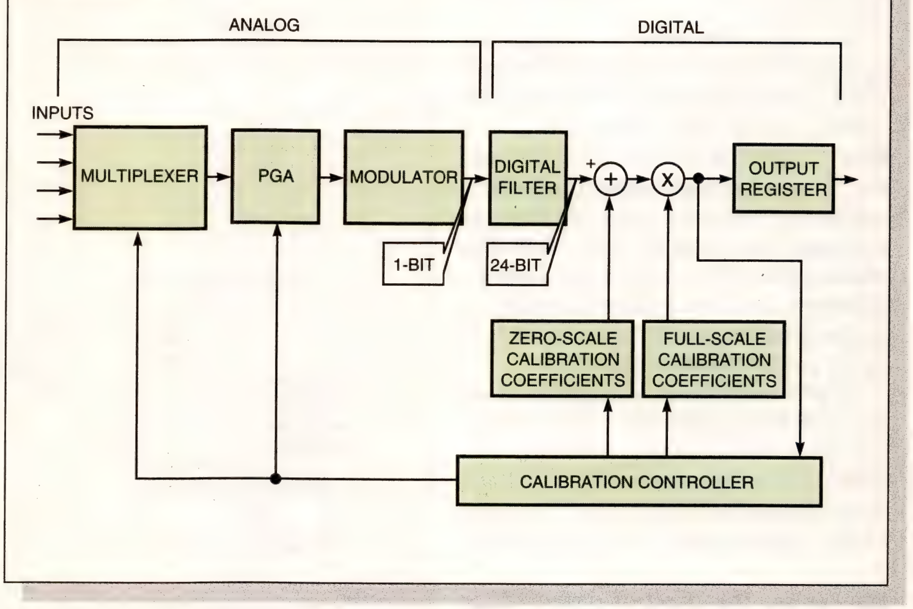
Converters implement calibration using either analog or digital techniques, depending on the internal architecture. Sampling converters are more compatible with calibration in the analog domain, and sigma-delta converters suit calibration in the digital domain.

In **Fig 2**, the sampling converters contain a capacitor DAC architecture, rather than a conventional R-2R ladder structure. When the device performs a calibration, the calibration controller in the digital section of the ADC adjusts the analog section of the ADC.

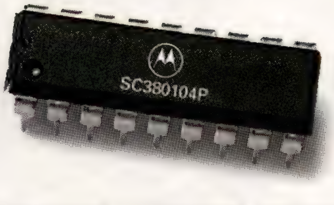
In contrast, the sigma-delta converter core is a 1-bit converter with a modulator that produces serial data. The modulator feeds the data into the digital filter. The converter designer can easily use some of the digital circuitry to perform calculations related to the calibration (**Fig 3**). As in the sampling converter, the calibration controller is part of the digital section of the ADC.

Although the two converter archi-

FIGURE 3



A sigma-delta ADC shows that most of the calibration-related circuitry consists of registers for storage of coefficients.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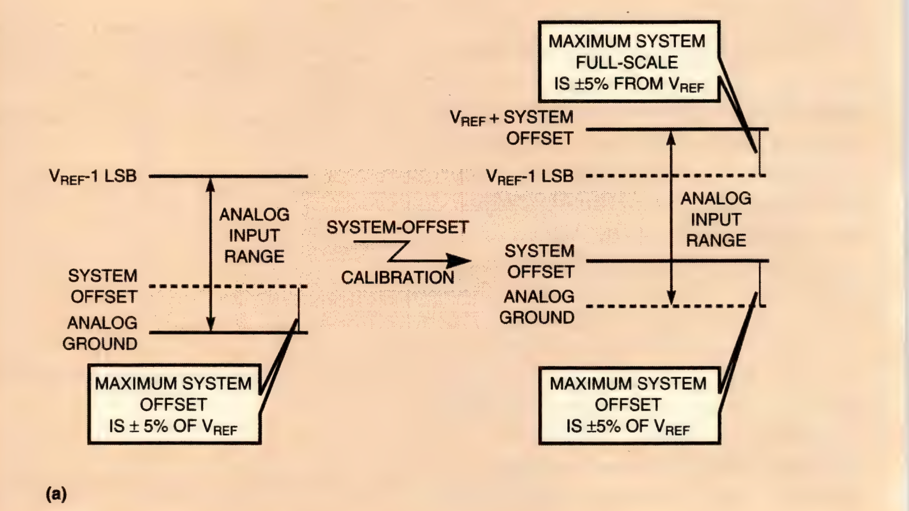
tectures differ in performing calibrations, they provide similar calibration options. In addition, most sigma-delta converters have a background-calibration feature.

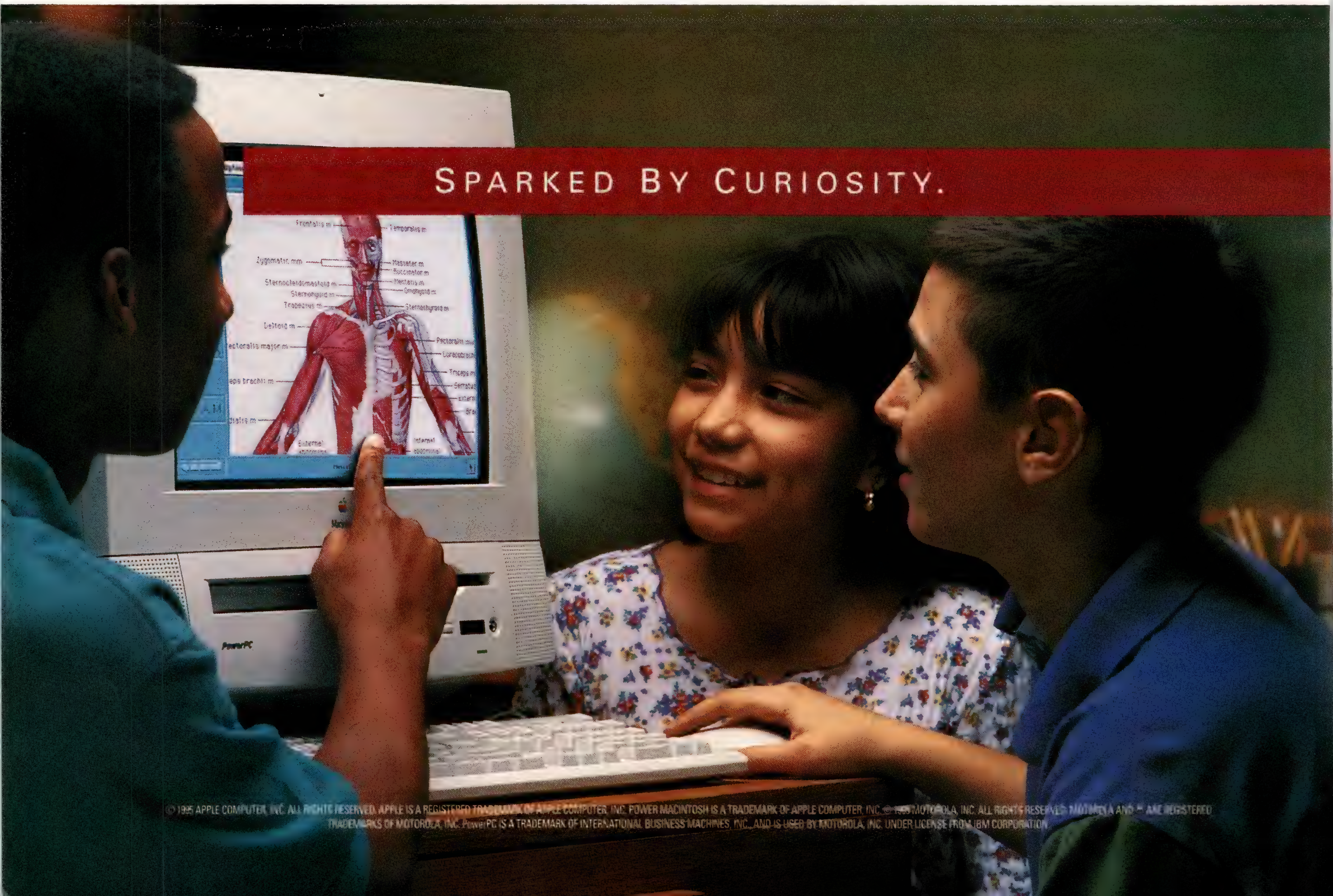
In a self-calibration, or device calibration, the part uses its own internal voltages to perform the calibration. In system calibration, in contrast, you have to provide the required voltages for the calibration sequence. System calibration takes out errors in the analog signal path and the ADC. Self-calibration takes out only the ADC errors. However, a self-calibration is easier to implement because you do not have to apply any external voltages.

In self-calibration, the part uses an internal voltage for the offset voltage (in most cases, analog ground). You must apply the system-offset voltage across the analog input pins in system-offset calibration. This calibration

FIGURE 3


MAXIMUM SYSTEM FULL-SCALE IS ±5% FROM V_REF
V_REF + SYSTEM OFFSET
V_REF-1 LSB
ANALOG INPUT RANGE
SYSTEM OFFSET
ANALOG GROUND
MAXIMUM SYSTEM OFFSET IS ± 5% OF V_REF
SYSTEM-OFFSET CALIBRATION
V_REF-1 LSB
ANALOG INPUT RANGE
SYSTEM OFFSET
ANALOG GROUND
MAXIMUM SYSTEM OFFSET IS ±5% OF V_REF
(a)

You can see the effect of system-offset (a), system-gain (b), and system-offset-plus-gain calibrations (c).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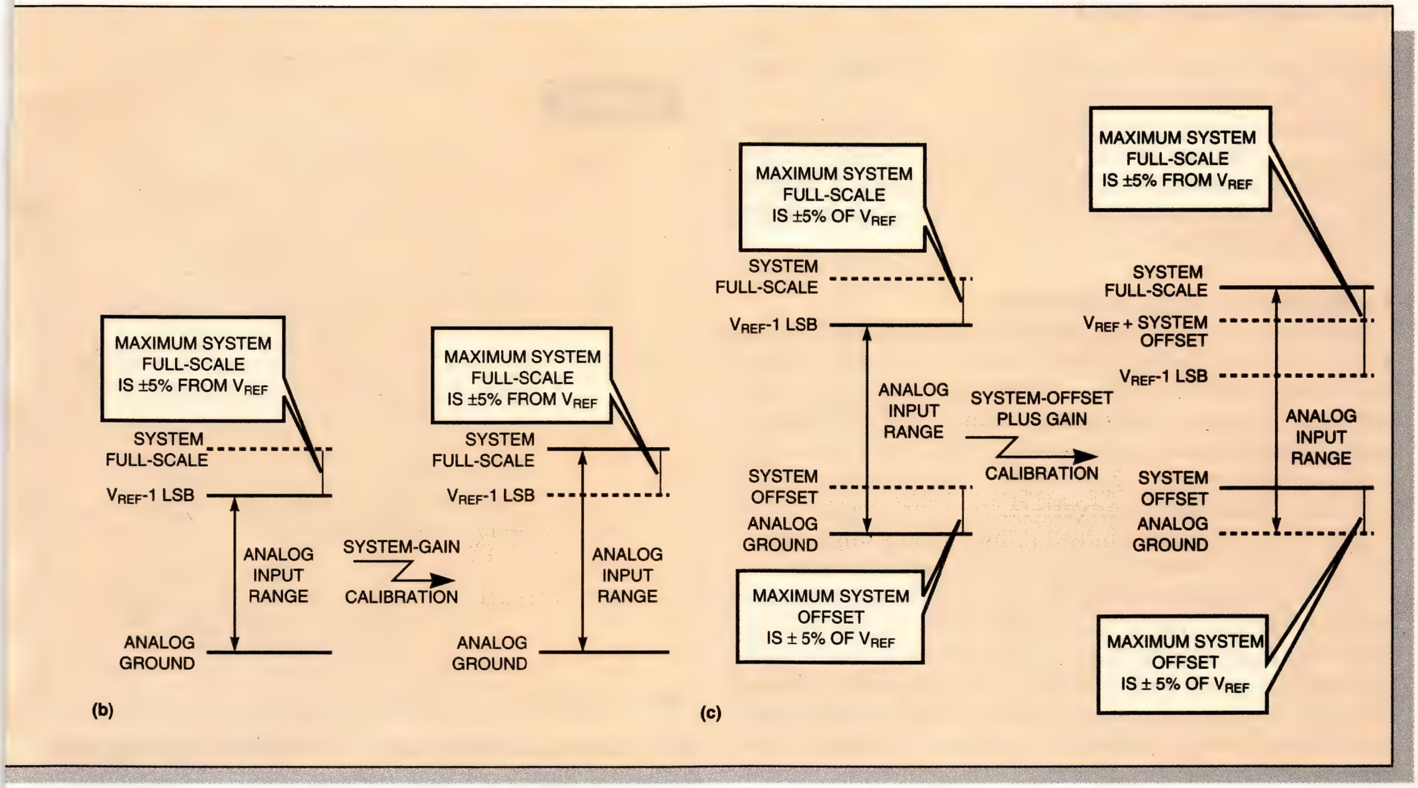
MAXIMUM SYSTEM FULL-SCALE IS ±5% FROM V_{REF}
SYSTEM FULL-SCALE
V_{REF}-1 LSB
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ANALOG GROUND
SYSTEM-GAIN CALIBRATION
MAXIMUM SYSTEM FULL-SCALE IS ±5% FROM V_{REF}
SYSTEM FULL-SCALE
V_{REF}-1 LSB
ANALOG INPUT RANGE
ANALOG GROUND
(b)
MAXIMUM SYSTEM FULL-SCALE IS ±5% OF V_{REF}
SYSTEM FULL-SCALE
V_{REF}-1 LSB
ANALOG INPUT RANGE
SYSTEM OFFSET
ANALOG GROUND
MAXIMUM SYSTEM OFFSET IS ± 5% OF V_{REF}
SYSTEM-OFFSET PLUS GAIN CALIBRATION
MAXIMUM SYSTEM FULL-SCALE IS ±5% FROM V_{REF}
SYSTEM FULL-SCALE
V_{REF} + SYSTEM OFFSET
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MAXIMUM SYSTEM OFFSET IS ± 5% OF V_{REF}
(c)

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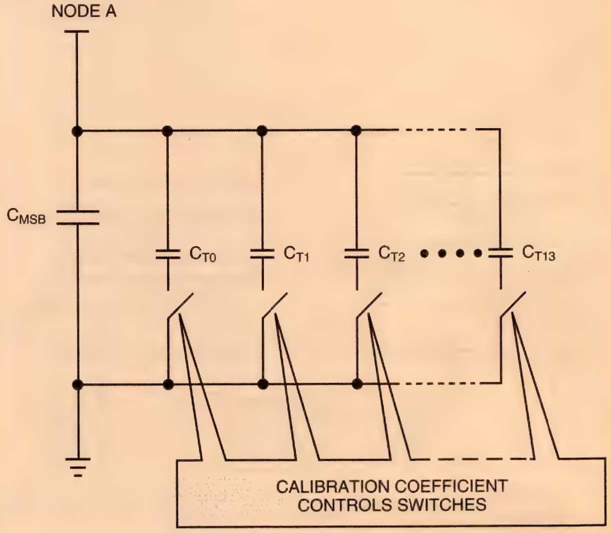
ensures that when you apply this offset to the input, the output of the converter is all 0s (zero scale).

System and self-calibrations provide you with three core features: calibration of the internal DAC; offset, or zero-scale, calibration; and gain, or full-scale, calibration. Various combinations of these core features provide different types of calibration (**Fig 4**).

Calibration reduces error source

Internal-DAC calibration reduces errors and improves the DAC linearity and accuracy. For sampling converters such as the AD7851/3/4/8/9 and the AD7882, each capacitor of the internal DAC has its own capacitor trim array (**Fig 5**). Switching the capacitors in the capacitor trim array in or out adjusts each capacitor, starting with the MSB and continuing to the LSB. For sigma-delta converters, such as the AD7710/1/2/3/4, linearity is determined primarily by a single capacitor, so no calibration is needed for improving linearity.

FIGURE 5



Trim arrays for sampling converters consist of capacitors that can be individually switched in or out; the offset and gain trim arrays are similar except they do not have the fixed MSB capacitor.

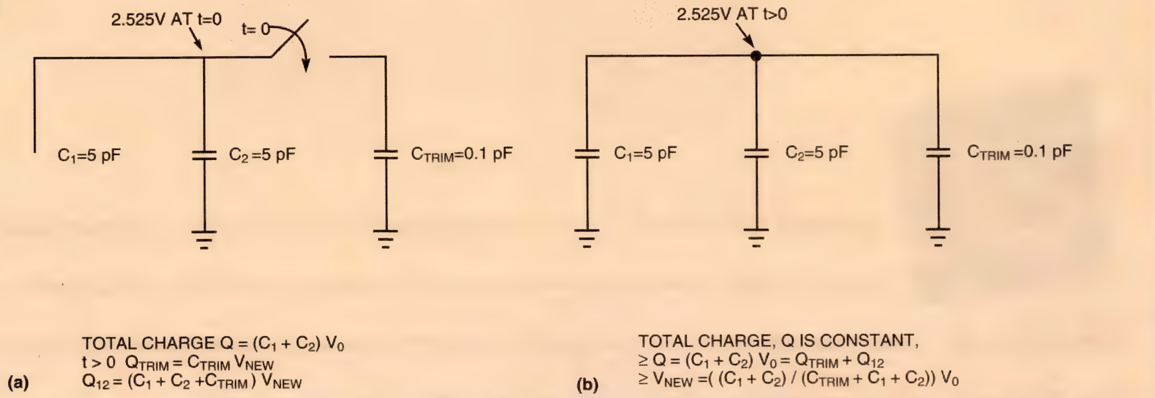
Gain calibration corrects the error at full scale. One reason to preform a system-gain calibration is because the system's full-scale voltage may be different from the voltage that the converter normally uses. For example, the normal full-scale voltage for many converters is the reference voltage. Another reason for doing a system-gain calibration is to remove reference errors, whether from an internal or external reference.

After you've completed gain calibration, the output of the converter is all 1s when you apply a full-scale voltage. For converters with multiple gain ranges, such as the AD771X family, you must perform a gain calibration at the different gains. When you are performing a calibration, the internal programmable-gain amplifier is set at a specific gain—the gain at which the calibration is to be performed. For example, for a self-gain calibration at a programmable gain amplifier (PGA) gain of 128, the part provides an input full-scale voltage of $V_{REF}/128$ to the input of the PGA, where this $V_{REF}/128$ is generated internally using a digital subsampling technique. With a 2.5 reference voltage, the internal calibration voltage has a 20-mV nominal value.

You can use system calibration to tailor the ADC for your application. You can remove offset and gain errors in the analog signal in the system software. However, this removal requires extra software-development effort. A self-calibrated converter, in contrast, eliminates the development effort and the recurring load on the processor, which can become significant at higher sampling rates.

Correcting linearity errors associated with the ADC in your processor requires a significant amount of software and

FIGURE 6


2.525V AT t=0
t= 0
C_1=5 pF
C_2=5 pF
C_{TRIM}=0.1 pF
TOTAL CHARGE $Q = (C_1 + C_2) V_0$
$t > 0$ $Q_{TRIM} = C_{TRIM} V_{NEW}$
$Q_{12} = (C_1 + C_2 + C_{TRIM}) V_{NEW}$
(a)
2.525V AT t>0
C_1=5 pF
C_2=5 pF
C_{TRIM} =0.1 pF
TOTAL CHARGE, Q IS CONSTANT,
$\geq Q = (C_1 + C_2) V_0 = Q_{TRIM} + Q_{12}$
$\geq V_{NEW} = ((C_1 + C_2) / (C_{TRIM} + C_1 + C_2)) V_0$
(b)

This shows calibration using charge-balance operation before (a) and after (b) the trim capacitor is switched in.

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effort to design, implement, and execute. It is easier for you to use the ADC to perform the offset-, gain-, and linearity-error corrections. Some errors, such as crossover distortion in audio applications and dead bands in the transfer function of control systems, are difficult to correct in a system processor. The ADC can remove these errors more effectively by using the full analog input range of the ADC to convert the analog signal.

Sigma-delta converters

Sigma-delta converters differ from sampling converters only in the internal DAC portion of full calibration. The converters often have an extra feature called background calibration, which works differently for each device. For example, for most members of the AD771X family, background calibration alternates between self-offset calibration and self-gain calibration after every conversion. This feature allows the device to remove the effects of temperature drift, supply sensitivity, and time drift on the offset and gain of the part

In contrast, background calibration on the AD7714 provides just a self-offset calibration after every conversion. You need to explicitly execute a separate self-gain calibration to remove the gain errors.

The internally stored calibration coefficients have different meanings in sampling converters compared with sigma-delta converters. For sampling converters, calibration coefficients are binary numbers that represent the state of various capacitor trim arrays on the device. The nominal valu all the calibration coefficients is one-half 1s and one-hal so that 50% of the capacitors in each of the trim array switched in. This initial position allows for an equal incr and decrease in the capacitance of each DAC, offset, and capacitor.

For sigma-delta converters, the calibration coefficient not control any physical switches or capacitors. Inst these coefficients numerically represent the errors due t offset and gain. The offset calibration coefficient is subt ed within the converter from the word (typically, 24 long for the AD7714) coming from the digital filter. gain-calibration coefficient is then multiplied by this r to give the final digital result that appears at the outpu

You can read or overwrite the calibration coefficient most converters with calibration. Reading allows yo check how far off your converter is, which detects any malfunctions of the converter or signal path, and to c on the actual span of your analog signal. Writing to the ibration registers lets you alter the calibration coeffic and, thus, tailor them for a specific application. For e ple, you may have an offset or gain error (or both) in system. Yet, you may not want to include extra circuitr switching in the system offset and gain voltages.

Your system does not have to go into calibration mo each power-up or reset. You can design your system so

(continued on p

INTERNAL CALIBRATION IMPLEMENTATION

The internal circuitry that implements calibration is different for sampling ADCs and sigma-delta ADCs. In sampling converters, such as the AD785X series, the internal DAC is calibrated by switching in or out capacitors in a capacitor trim array. The absolute values of the capacitors, which are difficult to control in IC fabrication, are not critical. The ratio of the various capacitors to each other in the DAC is critical, however, because mismatch in the capacitors produces calibration errors. Fortunately, this ratio is much easier to control.

The calibration controller determines how many capacitors in each trim array need to be switched in or out. Charge in the DAC is constant for a given input voltage, and, when the input voltage is sampled, a charge balance takes place. This charge balance serves as the basis for internal calibration. All the capacitors in the DAC have one end connected to a common node and the other to analog ground (node A for **Figs 2** and **5**). The common node is connected to the input of a comparator, and the calibration controller reads the output of this comparator.

When the converter performs calibration, the input of the comparator must be at a certain voltage to ensure that the capacitors being compared are matched. The calibration controller monitors the voltage on the common node, via the digital output of the comparator. Because the charge is constant, the voltage on the common node can be reduced by switching in one of the capacitors, such as C_2, in the capacitor trim array associated with the capacitor (**Fig 6**).

The calibration controller initially samples 5V on C_1 alone. If C_1 and C_2 were perfectly matched, the voltage would be 2.5V after the charge distribution. Instead, the voltage on the common node is at 2.525V, so the capacitor from the capacitor trim array is switched in, and the charge gets distributed to the trim capacitor (CTRIM) and capacitors C_1 and C_2. The charge balance that occurs reduces the voltage on the c mon node to 2.5V, so the capacitor and C_2 match.

The controller needs to switch out trim capacitor to increase the voltag the common node. This switching c not alter the voltage because the ch is lost by disconnecting the CTRIM, the input voltage is sampled ag There are now fewer capacitor charge than before, so the voltage the common node increases comp with when the CTRIM was previo switched in.

For the sigma-delta converters, n of the calibration implementation is ital. The main functional blocks rel to calibration are the adder, multip and calibration controller. You can instruct the system processor to dir read or write the registers that store calibration coefficients, to overrid crosscheck any calibration values d mined by the converter itself.

SPECIAL ADVERTISING SECTION

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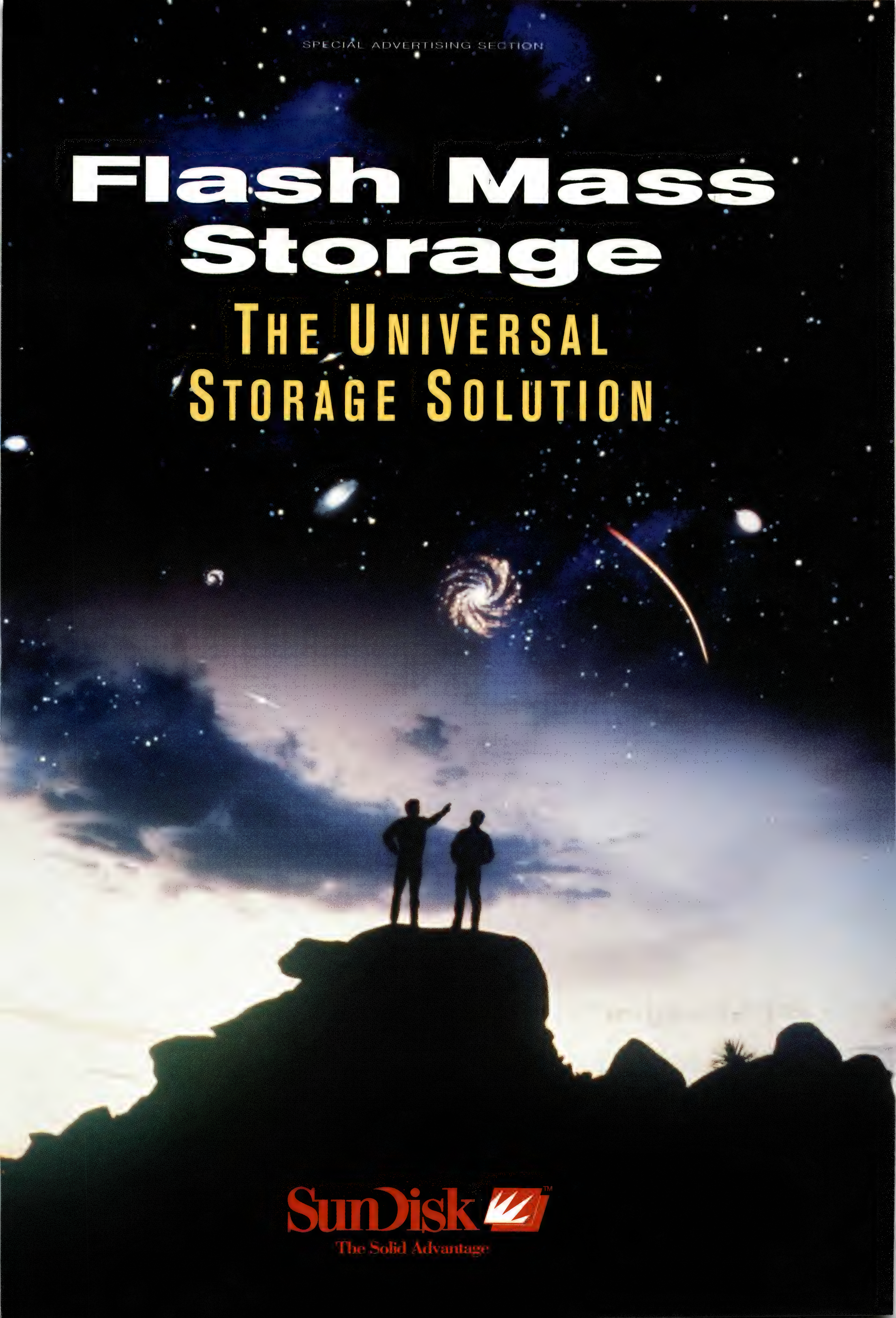


SunDisk™

The Solid Advantage

Flash Mass Storage:

the *universal* storage solution

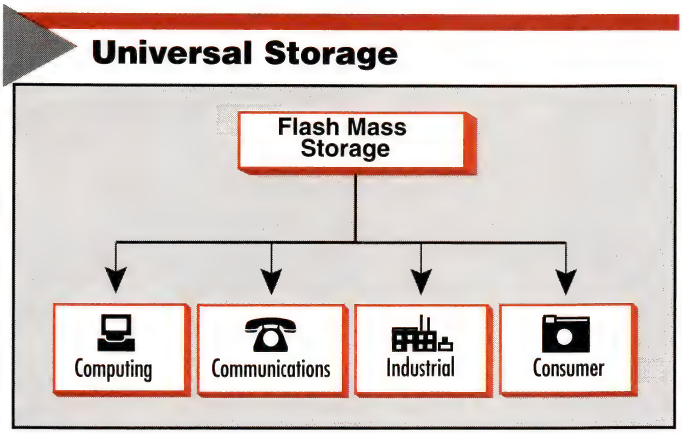
Flash mass storage outstrips all other memory technologies for compatibility, ruggedness, reliability, capacity, smaller size and lower power consumption. And one company has the enabling technology for industrial, consumer, computing and communications applications in the Flash mass storage marketplace: SunDisk.

Markets on the Move

In the 1990s, computing has become a pervasive phenomenon, expanding beyond the boundaries of desktop, notebook and mobile PCs to encompass a wide range of portable digital devices for communications, consumer electronics, computing and industrial applications. These devices include an expanding array of handheld data collection and inventory systems, pagers, cellular phones, embedded controllers, medical monitors, and navigation systems. In addition, a range of other compact, mobile electronic products continue to broaden our productivity, efficiency and application horizons.

These devices face a specific shared set of challenges that are markedly different from those faced by desktop computers. They require information storage devices that can withstand rough handling. They must be capable of operating for many hours with minimal power consumption, often relying on just two AA batteries which must be used for extended periods of time without recharging. They must provide a way to easily exchange information between each other and a variety of systems including the desktop PC. And, they must offer compact size and small form factors, while at the same time keeping pace with application demands by extending their memory capacities to store increasing amounts of data.

Standard rotating hard disk drives, while ideal for office and desktop environments, are not a feasible alternative for many of today's portable, handheld, communications and industrial applications. Hard disk drives employ rotating media with moving, mechanical parts. Because of this, they are not rugged enough to perform reliably under the various environmental conditions (shock, vibration, temperature, humidity, altitude, etc.) that many of today's applications


Universal Storage

must contend with. In addition, even the most energy efficient rotating disk drives consume approximately ten times more power than solid-state memory, quickly drawing down the battery charge of portable equipment.

To meet these requirements, some system designers have turned to static random access memory (SRAM) technology. But SRAM memory cards require built-in batteries limited to a shelf life of only a year or so; when the built-in battery dies, all data contained on the card is lost. SRAM capacities rarely exceed 1 MB in real-world application usage, due to the high cost of SRAM implementations.

There is one data storage technology, however, whose characteristics and features fit the requirements of the portable digital device. That technology is Flash mass storage—tailored specifically for low-power, portable, data-intensive applications that must withstand a variety of rugged environmental conditions. Flash memory is non-volatile, enabling it to retain indefinitely any files written into it. No battery is required to retain stored data, and minimal power is drawn from the host computer essentially only during read or write operations.

Flash Mass Storage: Beyond Linear Flash

Flash memory first appeared in the industry in the late 1980s, and soon made its mark as a viable alternative to ROM and EPROM memory implementations because of in-system reprogrammability. Flash currently offers lower cost and higher capacity when compared to SRAM memory solutions. Flash price is also dropping well below the cost of DRAMs.

Today, there are two types of Flash memory technology in the market: one is socket Flash (which, when used in memory cards, are called linear Flash cards), while the other is Flash mass storage. There are significant differences between the two.

Socket Flash—designed initially to be a socket replacement for standard EPROMs—is delivered in the form of a memory chip embedded in the system.

This chip stores the computer's firmware (operating systems, system BIOs, etc.), much of which typically needs to be updated—i.e., erased and written to infrequently.

While socket Flash is appropriate for "read mostly" operations, significant problems arise when socket Flash chips are used in memory cards as a mass storage device. Typically partitioned into 64KB blocks, all bits in one block are erased simultaneously and the erase time is slow—typically one second. DOS files on the other hand are stored in 512 Byte blocks

which is the size of a sector on a rotating disk drive. In addition, manufacturers of linear Flash cards employ different proprietary architectures to write and erase their Flash chips.

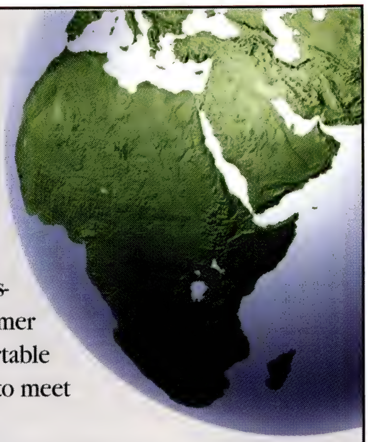
As a result, linear Flash cards have a difficult time trying to emulate the mass storage function of a disk drive, are not fully DOS compatible or platform independent, and exhibit dramatic performance degradation when filled close to maximum capacity.

By comparison, Flash mass storage solutions from SunDisk Corporation are based on an architectural approach targeted at applications that feature a high incidence—sometimes ranging into the hundreds of thousands—of memory erases and writes. This ability makes SunDisk's Flash mass storage a superior alternative to linear Flash for dynamic, data-intensive applications, where information is frequently being changed and updated.

SunDisk's Flash chips are built using 512 Byte data sectors, each of which can be individually erased in as little as one millisecond—significantly less than the 10 milliseconds latency typically found in rotating disk drives. Because of this, SunDisk's controller completes a sector erase operation as part of each write operation without significantly impacting performance. By partitioning the Flash arrays into 512 Byte sectors, 100% DOS compatibility and full emulation of the industry-standard file structure for disk drives are achieved.

In addition, SunDisk's Flash mass storage offers substantially higher storage capacities compared to any other Flash solution, ranging from 1.8 MB to as high as 175 MB. Stacker™ data compression software is available as an option, and effectively doubles these capacities up to 350 MB. And SunDisk's Flash mass storage doesn't share linear Flash's incompatibility and interface problems. Designed to comply with the PC Card ATA industry standard and provide forward and backward compatibility with previous and future generations, SunDisk's Flash mass storage offers a degree of flexibility, interoperability and data reliability that is unmatched by any other mobile mass storage solution.

A World of Applications



Flash mass storage is a non-volatile, rugged, reliable, compact, high-capacity, low-power data storage technology, making it ideal for systems that must withstand physical abuse and operate under low power. A range of industrial, medical, avionics, point-of-sale, consumer electronics, communications and other portable applications are now using Flash solutions to meet their highly specific requirements.

SunDisk's customers provide a wealth of application examples. The company's Flash mass storage products are now being employed in a range of in-flight computer systems, and are being designed into navigation systems for automobile and marine applications. A number of OEM customers have designed SunDisk Flash mass storage solutions into handheld terminals intended for use in inventory control, field data collection and scanner applications. Heart monitors and other medical systems employ the technology to allow patients to record and monitor their own health status rather than having to go to the hospital. Global communications companies are using SunDisk solutions for cellular switching and PBX stations, and networks are using them for software configuration and upgrades. And the technology is seeing widespread use in a range of trucking, railway and farm equipment applications for diagnostic, GPS and routing systems.

Whether implemented as an embedded drive (FlashDrive) or a removable PC Card ATA card (FlashDisk), SunDisk's mass storage solutions offer business card-sized form factors that are ideal for the ever-shrinking portable applications arena. FlashDisks enable users to store all of their information files—data, voicemail, video clips, e-mail, photographs and images, for example—on a portable device small enough to fit in a pocket. And SunDisk's new matchbook-sized CompactFlash cards have emerged as an ideal storage solution for small-form-factor systems that need high capacity, removable mass storage and PCMCIA connectivity, but are too small to accept a standard-size PC card. These include such emerging applications as film for digital cameras, fax capability in cellular phones, voicemail in pagers, audio recorders, personal communicators, musical instruments and interactive TV set-top boxes.

ATA vs. Non-ATA

ATA
(SunDisk FlashDisk)

- Open industry standard
- Guaranteed forward & backward compatibility
- Guaranteed interoperability
- Guaranteed reliability

Non-ATA
(Linear Flash Cards)

- Closed proprietary architecture
- Compatibility issues
- Reduced performance

SunDisk: The Flash Mass Storage Pioneer

No company has had a bigger impact on extending the frontiers of Flash mass storage technology and its applications than SunDisk Corporation. Based in Santa Clara, CA, the privately held SunDisk has focused exclusively on Flash mass storage since its founding in 1988. This focus has enabled the company to become the world leader in the Flash mass storage marketplace.

According to market research firm BIS Strategic Decisions, SunDisk shipped 41% of all worldwide Flash mass storage cards in 1994—almost three times the amount of its closest competitor.

SunDisk's sole focus has always been on Flash mass storage technology, which enables the company to move quickly from one generation of Flash mass storage solutions to the next. SunDisk has concentrated on developing a unique data storage subsystem based on the combination of proprietary Flash technology—developed from the ground up—and a unique controller architecture.

Intelligent Controller: Compatibility and Ease of Use

Compatibility with industry standards is a significant issue in the marketplace. Linear Flash cards will operate only on computers that use the same read/write algorithms as the host system on which the Flash card was originally used. By contrast, SunDisk's Flash cards are "plug and play" solutions that provide true host independence, enabling them to be used with any computer that supports the PC Card ATA standard—regardless of which host CPU or operating system is employed. This interoperability is due to the fact that the intelligent controller onboard the SunDisk card organizes the Flash chips to appear to the host CPU as though they were a disk drive, eliminating the need for special driver software and establishing complete compatibility with virtually all of today's leading operating systems.

SunDisk Industry Firsts in Flash

FlashDrive
First 1.8" IDE Drive
(1991)

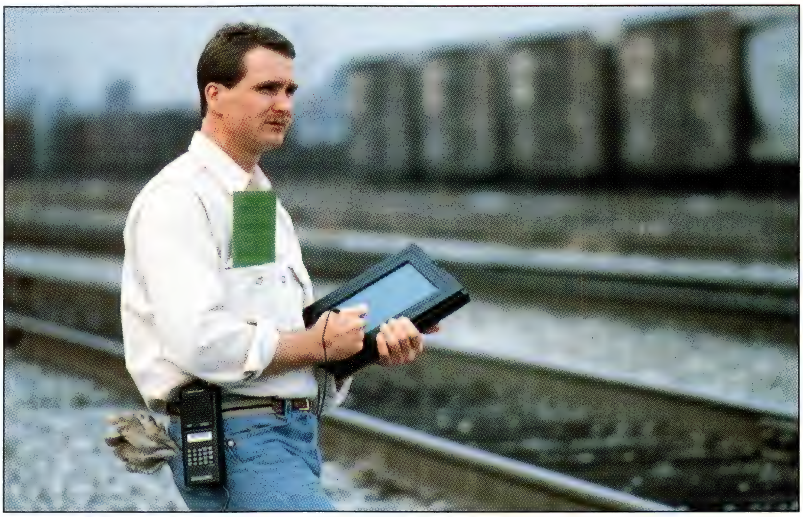
FlashDisk
First Type II 20 MB
PC Card ATA Card
(1992)

FlashDisk
First Type II 40 MB
PC Card ATA Card
(1993)

FlashDrive
First 1.3" IDE Drive
(1994)

FlashDisk
First Type III 175 MB
PC Card ATA Card
(1995)

CompactFlash™
Smallest Removable
Flash Storage Device
(1995)



Equally important, SunDisk's intelligent controller allows the Flash cards to be forward and backward compatible, enabling them to interoperate seamlessly from one generation to the next. For example, any of today's SunDisk FlashDisks can be inserted into any future system that complies with the PC Card ATA standard. And any future generations of SunDisk products will work flawlessly with older systems that comply with the ATA standard.

SunDisk's proprietary intelligent controller performs all data management functions. The controller's dynamic defect management and error-correction code (ECC) safeguards the integrity of data, providing the ability to discover and replace defective bits in a way that is transparent to the host and does not consume any user data space.

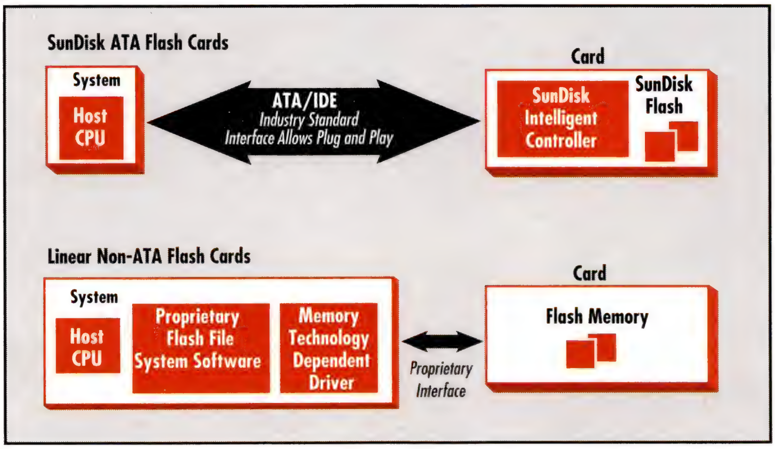
As a result of these innovations, SunDisk's unique, patented hardware implementation is much faster and far more reliable when compared to linear Flash, where the majority of cards provide no protection against failing bits and no ability to recover lost files.

Additionally, SunDisk's intelligent controller provides system power management techniques that put the card into a very low-power "sleep mode" any time the card is not being accessed by the host system, thus greatly conserving system battery life.

SunDisk: Products for Universal Storage

SunDisk currently offers three distinct Flash mass storage product lines: the PCMCIA (Personal Computer Memory Card International Association) FlashDisk series, the CompactFlash™ (CF™) series and the IDE FlashDrive series—all of which share the same high-density, proprietary SunDisk Flash memory chips, as well as the same intelligent controller. All SunDisk products meet industry standards and provide superior compatibility via host independence. All offer complete forward and backward compatibility from one generation to the next. And each product is highly reliable: FlashDisks, FlashDrives and CompactFlash cards all offer a mean time between failures (MTBF) rate of 500,000 hours—which translates to more than 100 years of standard operation.

ATA vs. Linear Flash Card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Host CPU
ATA/IDE
Industry Standard
Interface Allows Plug and Play
Card
SunDisk Intelligent Controller
SunDisk Flash
Linear Non-ATA Flash Cards
System
Host CPU
Proprietary Flash File System Software
Memory Technology Dependent Driver
Proprietary Interface
Card
Flash Memory

In addition, all three SunDisk product families are offered with a Stacker™ compression option that effectively doubles storage capacity. All SunDisk products are available in industrial (-25°C to +75°C) and commercial (0°C to +60°C) temperature operating ranges. All SunDisk products operate from a single 5V supply. The CompactFlash series also supports operation from a single 3.3V supply.

• PCMCIA FlashDisk Series

SunDisk's FlashDisk products, used in storage, data backup and data transport applications, are the highest-capacity removable Flash mass storage PC Card ATA cards currently available. Type II FlashDisks range in capacity from 1.8 to 40 MB, while SunDisk's Type III cards offer capacities of 80,110 and 175 MB—setting new capacity standards in the industry. PC Card ATA standard support makes the FlashDisk series compatible with virtually all of today's computing and communications systems, supported by such varied operating systems as DOS, Windows, Windows 95, OS/2, NEC OS, DOS V, GEOS, PSOS and Apple System 7.

- **CompactFlash™ Series**

CompactFlash's matchbook size and half-ounce weight makes it the world's smallest removable mass storage system. Its compact size, ruggedness (an operating shock rating of 2,000 Gs—equivalent to a 10-foot drop onto concrete), and low-power, single-supply 3.3V features make CompactFlash ideal for a range of current and next-generation, small-form-factor consumer applications such as digital cameras, cellular phones, PDAs, personal communicators, pagers and audio recorders. CompactFlash provides complete PC Card ATA functionality and compatibility through a Type II PCMCIA adapter. CompactFlash is available in 2, 4, 10 and 15 MB storage capacities. The Stacker compression software option effectively doubles these capacities.

- **IDE FlashDrive Series**

SunDisk's 1.3" and 1.8" form factors are targeted at applications that require embedded mass storage. As such, IDE FlashDrives are ideal for mobile computers, communication devices and other embedded systems that require low power, high resistance to shock and vibration, instant access to data, and complete plug and play compatibility with IDE rotating disk drives without requiring any hardware or software modifications. IDE

Strategic Alliances: A Foundation for the Future

In today's global high technology arena, strategic alliances are necessary to achieve ongoing success. SunDisk is currently working closely with a number of industry leaders to solidify its leadership position and advance the frontiers of Flash mass storage technology.

Seagate Technology, a worldwide leader in data storage products, currently holds a 25% equity investment in SunDisk, providing the company with access to a wide range of industrial distributors. An alliance with Matsushita Electronics Corporation provides SunDisk with high-volume, advanced semiconductor development and manufacturing facilities, access to the Japanese consumer and communications markets, and shared research and development costs for ongoing product development. Japan's NEC and SunDisk are now involved in joint development of 256-megabit Flash mass storage solutions using 0.35-micron process technology, slated for production in 1997. And LG Semicon (formerly Goldstar) is currently producing SunDisk's 16 Mbit and 32 Mbit Flash chips.

In addition to these alliances, SunDisk is also engaged in numerous OEM sales and marketing agreements with companies such as Epson, Hewlett-Packard, Matsushita, Motorola, 3M and Verbatim. And distribution agreements with international distributors including Anthem, Arrow, Bell Microproducts, Hamilton/Hallmark, Avnet Computer and Prima International help to ensure that SunDisk's Flash mass storage technology and products are readily available in the global marketplace through multiple sales channels targeted at specific market segments.

FlashDrives feature capacities ranging between 4 and 80 MB. Stacker software is also available as an option.

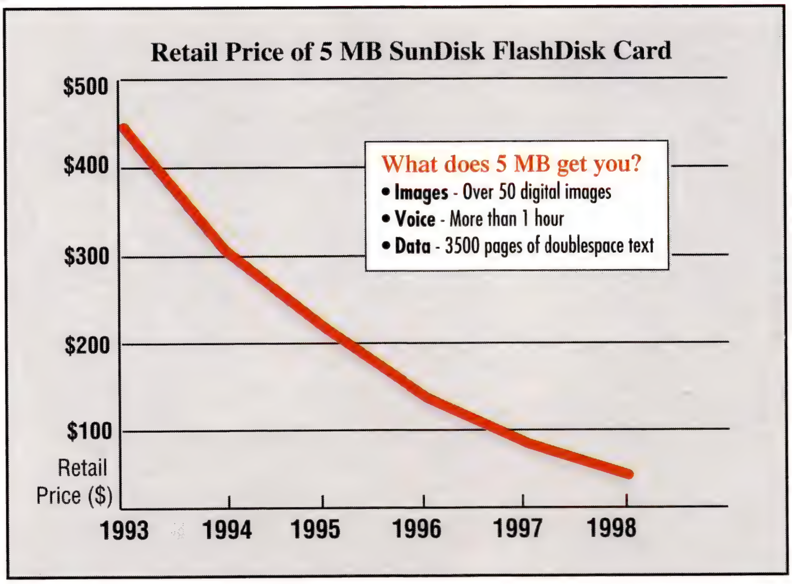
SunDisk: Commitment to Driving Prices Down

SunDisk's rapid technological advances have enabled the company to offer customers higher storage capacity for lower prices. This trend will continue. For example, a 5 MB FlashDisk PCMCIA PC Card ATA FlashDisk now retails for approximately $300; the same capacity is expected to retail for under $50 within the next three years, made possible by employing SunDisk's advanced Flash chips, which are currently under development. This continual decline in prices promises to significantly increase the impact this technology will have on the wide variety of applications in today's industrial, consumer, computing and communications marketplaces.

Flash to the Forefront

And as the frontiers of Flash mass storage continue to move forward, SunDisk will be there leading the way. When combined, all of SunDisk's architectural advantages —superior data reliability, low-power operation, outstanding resistance to shock and vibration, and small, lightweight form factors—is and will continue to enable customers around the globe to develop new product opportunities and applications.

Cost Trends



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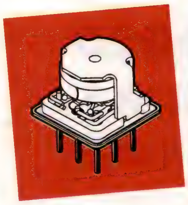

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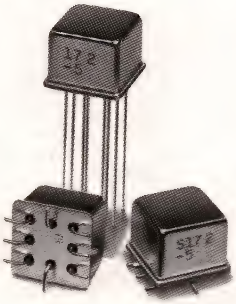

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CIRCLE NO. 31

the processor can read back calibration coefficients after initial factory calibration and store the coefficients in nonvolatile memory. The coefficients can then be downloaded to the device whenever the system is powered up. This readback is useful for applications in which the coefficients are automatically downloaded. Downloading the coefficients effectively performs a system calibration, invisible to the end user, to correct the analog signal and ADC errors.

Even calibration has its limits

System calibration has limitations. There is a limited amount of head room that vendors can build into the ADCs. Therefore, you have to ensure that the system-offset and system-gain errors are within a certain range of the nominal zero-scale and the nominal full-scale voltages.

Sampling converters, such as the AD785X series, have a system-offset error typically ranging from –0.05 to +0.05 V_{REF}. The system-input span range is 0.95 to 1.05 V_{REF}, due to the limited number of trim array capacitors. This limitation is physical because the converter manufacturers do not want a large number of capacitors on the IC taking up substantial silicon area. Because the silicon is the main constraint, the sampling converters can tolerate a smaller range for the system full-scale and system-offset voltages when compared with sigma-delta converters.

Sigma-delta converters have restrictions, but for a different reason. The converter's large tolerance range on input span and system-offset voltage exists because their head room is constrained primarily by digital circuitry and only partly by the analog circuitry. In converters such as the AD771X series, the system-offset range is from –1.05 to –0.95 V_{REF}, and the system-input range is from 0.4 to 1.05 V_{REF}. If the offset and gain errors are outside these ranges, the ADC reduces the errors as much as possible, but it may not reduce them fully. The AD7714, for example, can handle a system full-scale voltage that is up to 5% greater or 60% less than the nominal full-scale voltage or the reference voltage. EDN

Author's biography

Sean O'Leary is an applications engineer with Analog Devices Inc, Limerick, Ireland, where he has worked for 2 ½ years. His job entails product definition and software and ADC development. O'Leary holds a bachelor's degree in electronic engineering from University College Cork, County Cork, Ireland. In his spare time, he enjoys soccer, squash, and skydiving.

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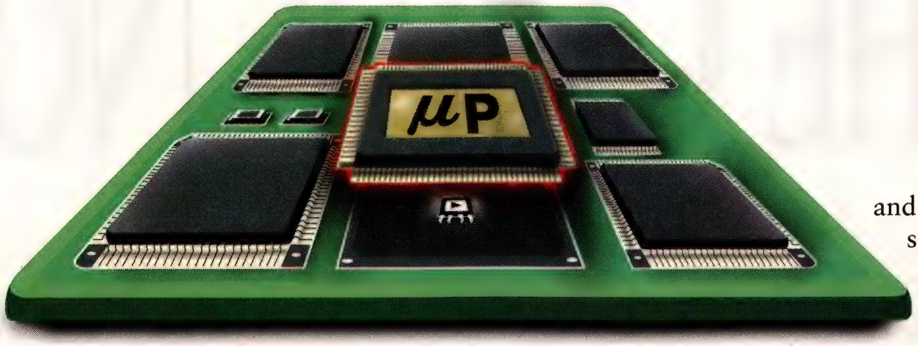

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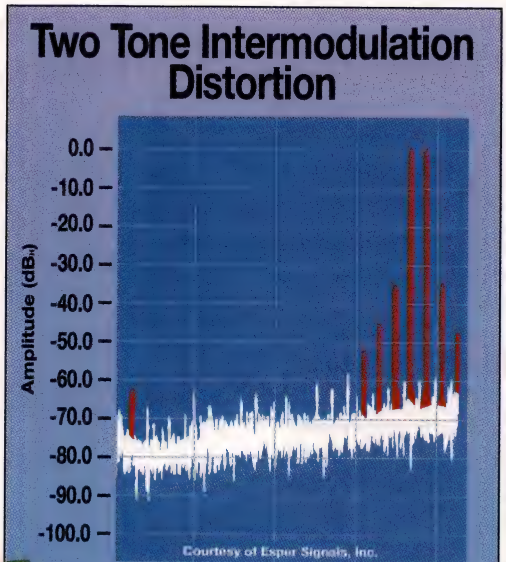

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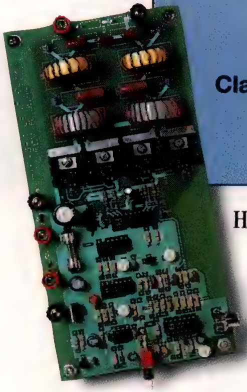

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CIRCLE NO. 153

Parallel-printer adapters find new use as instrument interfaces

DHANANJAY V GADRE, INTER-UNIVERSITY CENTRE FOR ASTRONOMY & ASTROPHYSICS

The venerable parallel-printer adapter has found many uses during its long lifetime. Now, you can use the port as an instrument interface—for connecting a photometer and a PC, for example.

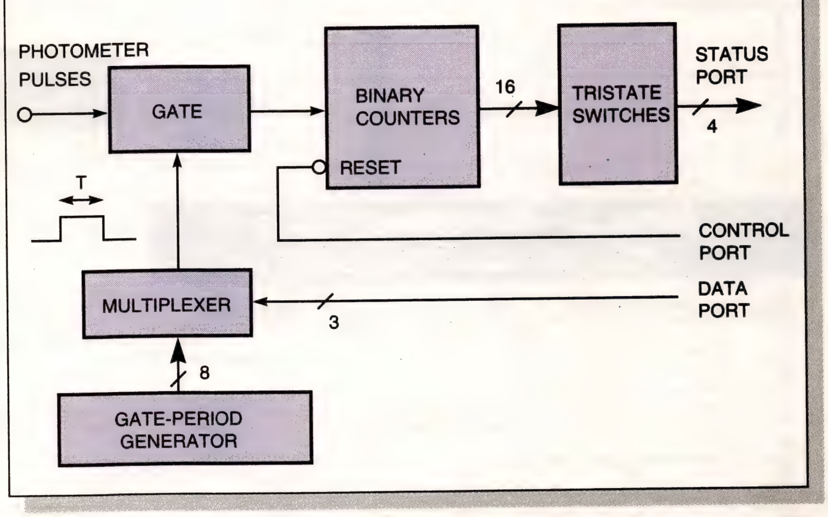
Designers of the Centronics, or parallel, printer adapter intended it as a way to connect printers and computers. However, the adapter's uses go far beyond simple peripheral connection. PC manufacturers have adapted the port for various applications on PCs, and, with decreasing hardware costs, PCs often have two or more parallel-printer adapters. In addition, the PC operating system, MS DOS, supports four printer adapters.

OEMs and instrument designers have also used the adapter for connecting devices other than printers to the PC (**Ref 1**). The adapter has enough I/O lines to be a fast communications channel between PCs and application hardware. Applications for the adapter include tape-backup systems, PROM programmers, ROM emulators, data-acquisition systems, and security locks. The parallel-printer adapter gives at least an order of magnitude improvement over the data-transfer rates you can achieve with the RS-232C port; the enhanced parallel-printer adapter does even better (**Ref 2**).

The adapter also helps avoid the problem of overcrowding motherboards with ISA/EISA add-on cards. Consider whether using the ISA or EISA bus in an instrument is overdesign. A printer adapter may work in these designs if other aspects, such as speed, are not a consideration. In addition, users cannot access the ISA bus in laptops, leaving the parallel-printer and PCMCIA adapters as the only available high-speed communication channels. (**Ref 2**).

Also competing with the parallel-printer adapter, the Enhanced Capabilities Port (ECP) and Extended Parallel Port (EPP) are beginning to appear on the market. However, the large user base of the standard parallel-printer adapter suggests that applications designed with it would have wider portability than that of ECP and EPP. An IEEE committee is now examining the parallel-printer adapter standard to compare its capabilities vs the ECP and the EPP (**Ref 2**).

FIGURE 1



The interface between a photometer and the parallel-printer port on a PC has a digital multiplexer that selects one to eight time periods. A binary counter divides down a 32.768-kHz crystal oscillator to set the gating periods from 0.125 to 16 sec in steps of 0.125 multiplied by powers of 2.

The printer adapter has three independent, TTL-compatible ports: an 8-bit output-data port, a 4-bit output-control port with open-collector drivers, and a 5-bit input-status port. The two output ports have input registers at identical addresses. You can read these registers to get the latched value. The control-port outputs have open-collector drivers with typically 4.7-kΩ pull-up resistors. The control port can also be used as an input port, by writing ones to the control register and then performing a read operation.

The control register lets you connect one of the status-port pins to one of the PC interrupt-request lines. The data RAM of the PC stores the port addresses. **Tables 1**, **2**, and **3** show the pin position of the three ports of the adapter on the 36-pin Centronics connector on the printer end and the DB-25 connector on the PC end. They also show the corresponding bit locations in a bytewide register and the logic relationship between the register contents and the output pin. A true relation means that if the register contains a logic one, the output pin is also at a logic one. An invert relation indicates that, if the register bit contains a logic one, the output pin is at a logic zero.

Use the interface for a photometer

As an example of using a printer adapter port as an instrument interface, consider an application in which a computer interface for a photometer will perform photometric observations. The photometer produces low-pulse-width pulses whose frequency is proportional to the incident light intensity. Photometric observations involve accumulating the pulses for a required time period. You can achieve this task by gating a counter with a preset timer. The program in **Listing 1** on pg 104 demonstrates the workings of the photometer interface through the parallel-printer adapter.

TABLE 1—PIN CONNECTIONS FOR THE STATUS PORT

Bit	Centronics pin	DB-25 pin	Bit-to-pin relation
7	11	11	Invert
6	10	10	True
5	12	12	True
4	13	13	True
3	32	15	True
2	-	-	-
1	-	-	-
0	-	-	-

TABLE 2—PIN CONNECTIONS FOR THE CONTROL PORT

Bit	Centronics pin	DB-25 pin	Bit-to-pin relation
7	-	-	-
6	-	-	-
5	-	-	-
4	-	-	-
3	36	17	Invert
2	31	16	True
1	14	14	Invert
0	1	1	Invert

If you want many computers to share the photometer, use the printer adapter to connect the photometer to a PC. This approach avoids removing the computer interface from the computer and also works well if you plan to use a laptop computer. However, this approach can mean adding an extra power supply for the circuit. To address this penalty, you can use the RS-232C signal lines to power the low current requirements of the interface circuit.

Acquisition follows a series of events

Fig 1 shows how the parallel-adapter interface circuit operates. The digital multiplexer selects one of eight time periods. A binary counter divides down a 32.768-kHz crystal oscillator to set the gating periods from 0.125 to 16 sec in steps of 0.125 multiplied by powers of 2. A chain of binary counters count the incoming pulses for the duration of one gate period. One cycle of acquisition begins by selecting the required gate period and then resets the accumulating counters. The subsequent rising edge of the gate signal routes the incoming pulses to the counters. The falling edge of the gate period disables the AND gate, which freezes the accumulated count in the counters. The program now reads the counter contents, 4 bits at a time. Following this operation, another measurement cycle begins.

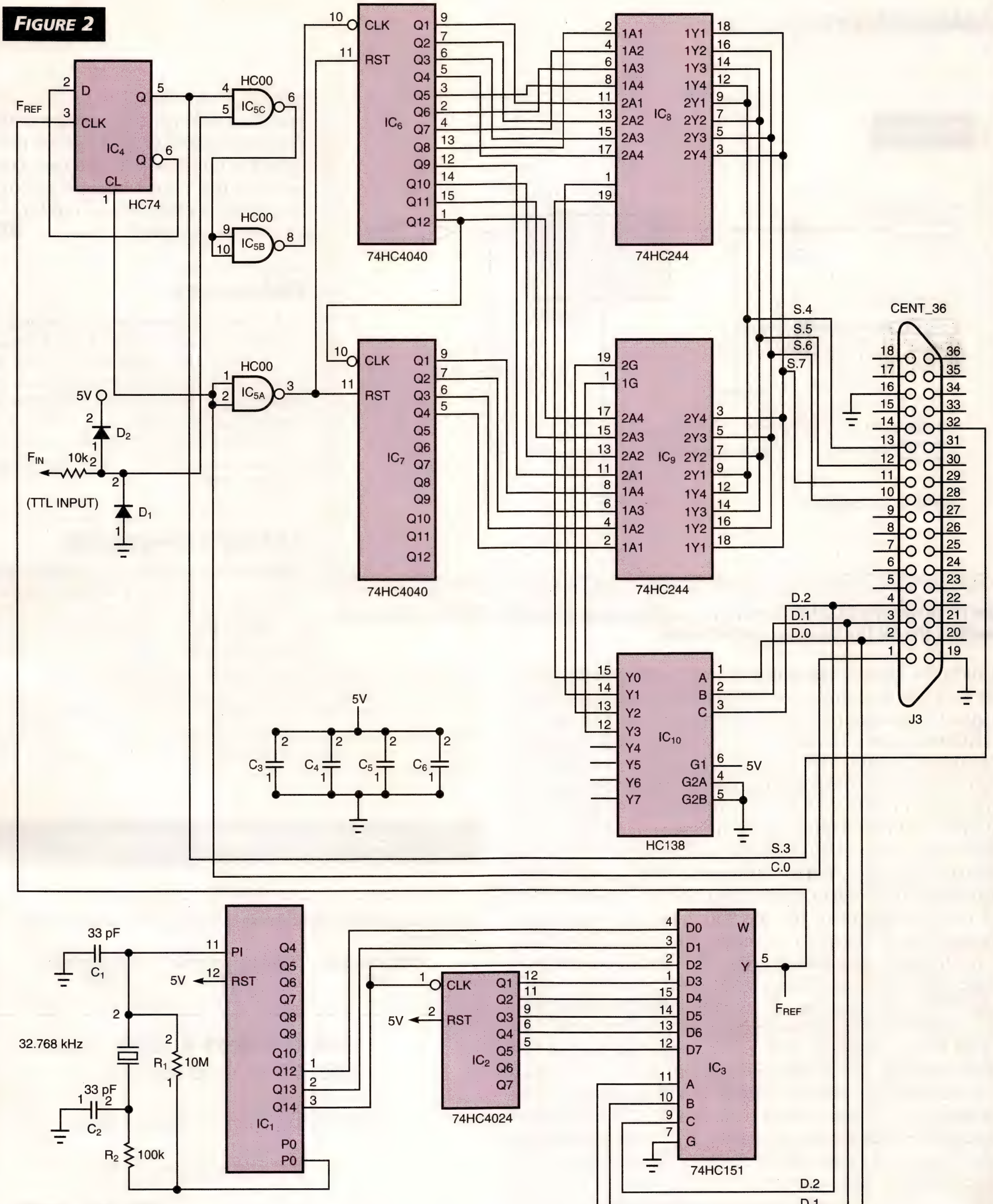
Fig 2 shows the acquisition circuit, which uses CMOS or 74HC components to keep the current consumption small enough for RS-232C signal lines to power the circuit. **Fig 3**

TABLE 3—PIN CONNECTIONS FOR THE DATA PORT

Bit	Centronics pin	DB-25 pin	Bit-to-pin relation
7	9	9	True
6	8	8	True
5	7	7	True
4	6	6	True
3	5	5	True
2	4	4	True
1	3	3	True
0	2	2	True

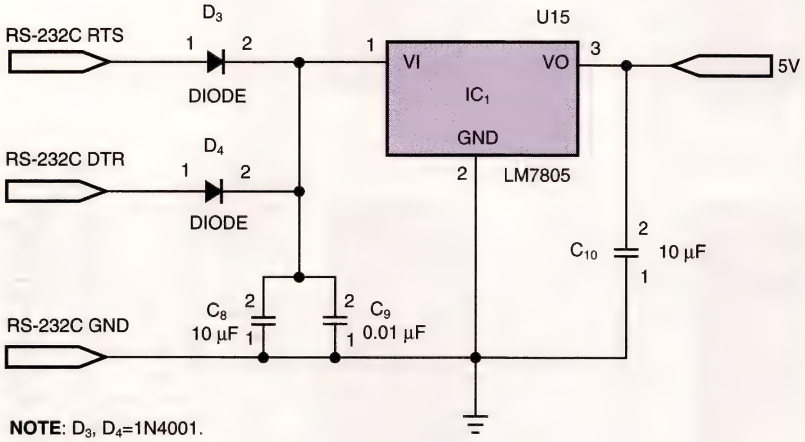
The acquisition circuit uses CMOS or 74HC components to keep the current consumption small enough for RS-232C signal lines to power the circuit. →

FIGURE 2



NOTES: D1,D2 = IN914
C3 TO C6 = 0.1 µF/16V
ALL RESISTORS: 1/4W, 5% CFR
ALL CAPACITORS: CERAMIC TYPE

FIGURE 3



The PC drives the RS-232C lines to V_{CC}, which passes through a 78L05 regulator to produce the 5V the interface circuit needs.

depicts the circuit's associated power supply. The PC drives the RS-232C lines to V_{CC}, which passes through a 78L05 regulator to produce the 5V the interface circuit needs. IC_1, 74HC4060, uses a 32.768-kHz crystal to generate the gating signal of ⅛, ¼, and ½ Hz. IC_2, 74HC4024, further divides this signal to generate the rest of the five periods. These eight gating signals drive IC_3, 74HC151, a one-of-eight digital multiplexer. The lower 3 bits of the printer-adapter data port act as the select input of this multiplexer. The output of the multiplexer drives IC_4, 74HC74, a D-type flip-flop in a divide-by-two mode, to generate signals with ON time from 0.125 to 16 sec. The output of the flip-flop gates the input pulses through the AND gates, IC_{5B} and IC_{5C}, to the counter chain.

During each acquisition cycle, the control-port bit, C0, resets flip-flop IC_4 and binary counters IC_6 and IC_7. A rising edge of the gate signal sets IC_4, enabling the incoming pulses to reach the binary-counter chain, IC_6 and IC_7, which are 12-bit binary counters. At the end of the gate period, the clock line to IC_4 freezes the accumulated count in the counters. The program can read only 16 bits (four nibbles) of the 24 bits output of these counters. IC_8 and IC_9, 74HC244, multiplexes the 16 bits to generate 4 bits. IC_{10}, 74HC138, decides which one of the four nibbles routes to the status port. The program reads the output of counters IC_6 and IC_7 4 bits at a time by reading the status port and manipulating the four nibbles to form a 16-bit integer.

The control program prompts the user to enter the required gate period and then starts acquiring data. The circuit stores the data as ASCII numbers in a user-defined output file at the end of the acquisition period. A suitable cable connects the photometer generating TTL-level pulses to the interface. The interface connects to the printer adapter through the 36-pin Centronics connector, J3, by the standard printer cable. EDN

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1. Gadre, Dhananjay V, Pramod K Upadhyay, and Vijaya S Varma, "Catching the right bus," Part 2: "Using a parallel-printer adapter as an inexpensive interface," *Computers in Physics*, January/February 1994.

2. Tracht, Allen E, "Adapting laptops to data acquisition," *IEEE Spectrum*, October 1993.

Author's biography

Dhananjay V Gadre is a scientific and technical officer for the Instrumentation Laboratory at the Inter-University Centre for Astronomy & Astrophysics in Pune, India, where he has worked for two years. He currently designs electronic instrumentation for use in astronomy. He is currently working on a controller for a low-noise (<5-eV) CCD camera. He is also helping in the development of a network of computer-controlled instruments on a client/server model. He has an MS in electronics from the University of Delhi in India and is a licensed radio amateur.

Turn to pg 104 for Listing 1.

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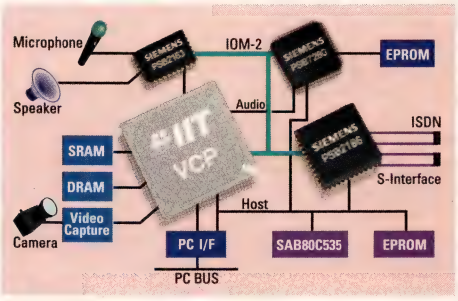

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LISTING 1—PHOTOMETER INTERFACE THROUGH THE PARALLEL-PRINTER ADAPTER

```
--------------------------------------------------------------------
/*****************************************************************/
/* Program to demonstrate the working of the Photometer interface */
/* through the parallel printer adapter. Connect the interface to */
/* LPT1 & COM1. Connect the photometer to the interface.         */
/*****************************************************************/
/*                 Compile with TurboC Ver. 2.0                  */
/*****************************************************************/


#include <stdio.h>
#include <dos.h>
#include <conio.h>
#include <process.h>


int modem_control_reg, dport_lpt1, cport_lpt1, sport_lpt1;

/* Declare the subroutines */
unsigned char get_integ_time(void);
unsigned int get_count(void);


unsigned char get_integ_time(void)
{
int temp;

clrscr();
printf("Character     Integration time\n");
printf("0             00.125 sec\n");
printf("1             00.250 sec\n");
printf("2             00.5   sec\n");
printf("3             01.0   sec\n");
printf("4             02.0   sec\n");
printf("5             04.0   sec\n");
printf("6             08.0   sec\n");
printf("7             16.0   sec\n");

temp=getchar();
switch(temp){
case '0':       return 0;break;
case '1':       return 1;break;
case '2':       return 2;break;
case '3':       return 3;break;
case '4':       return 4;break;
case '5':       return 5;break;
case '6':       return 6;break;
case '7':       return 7;break;
default:        return 100;

 }
 }


unsigned int get_count(void)
{
unsigned char monitor, nib_0, nib_1, nib_2, nib_3;

/* Reset the binary counters U6, U7 & the flipflop U4-A */
/* The Control port bit C0 of the printer adapter is used */
outportb(cport_lpt1,1);
outportb(cport_lpt1,0);


/* Monitor the o/p of flipflop U4-A */


/* Wait in the loop till it is zero */
monitor = 0;
while(monitor == 0) monitor = inportb(sport_lpt1) & 0x08;

/* Now the flipflop has enabled the counters */
/* So, wait till the counting is over  */
monitor = 0x08;
while(monitor == 0x08) monitor = inportb(sport_lpt1) & 0x08;

/* Read the four nibbles*/

/* Nibble 3, the most significant nibble*/
outportb(dport_lpt1,3);
nib_3 = inportb(sport_lpt1);

/* Nibble 2 */
outportb(dport_lpt1,02);
nib_2 = (inportb(sport_lpt1) >>4);

/* Nibble 1 */
outportb(dport_lpt1,1);
nib_1 = inportb(sport_lpt1);

/* Nibble 0, the lest significant */
outportb(dport_lpt1,0);
nib_0 =(inportb(sport_lpt1) >> 4);


/* put all the nibbles in one integer variable */

nib_1 = nib_1 & 0x0f0;
nib_1 = nib_1 | nib_0;

nib_1 = nib_1 ^ 0x88;

nib_3=nib_3 & 0x0f0;
nib_3 = nib_3 | nib_2;
nib_3 = nib_3 ^ 0x88;

/* Return the unsigned integer */
return (nib_3*256 + nib_1);
}


void main(void)
{
unsigned char int_win;

/* Sign ON */
clrscr();
printf("Photometer interface for the IBM PCs & compatibles, Version
1.0");
printf("\nUses the parallel printer adapter for counting");
printf("\n&the RS-232 port for the power supply");
printf("\n\nBy: D.V.GADRE");

/* Get COM1 register address */

modem_control_reg = peek(0x40,0)+4;
if(modem_control_reg == 4)
        {
        printf("\n\n\nCOM1 not available... aborting\n\n\n");
        exit(1);
        }
printf("\n\n\nCOM1 address = %X",peek(0x40,0) );

/*Get LPT1 port addresses */

dport_lpt1 = peek(0x40,0x08);
if(dport_lpt1 ==0)
        {
        printf("\n\n\nLPT! not available... aborting\n\n\n");
        exit(1);
        }
printf("\nLPT1 address = %X", dport_lpt1);
cport_lpt1 = dport_lpt1 +2;      /* control port address */
sport_lpt1 = dport_lpt1 + 1;     /* status port address */

/* put power On on COM1 */
outportb(modem_control_reg, 03);
printf("\nPutting Power ON...\n\n\n");
sleep(1);


/* Get the integration time window */
int_win = get_integ_time();

while(int_win<0 || int_win >7) int_win = get_integ_time();
clrscr();

printf("Using integration window %d\n\n", int_win);
while(!kbhit())
                {
                /* set integration time */
                outportb(dport_lpt1, int_win);

                /* Get the accumulated count & print it on the screen
*/
                printf("%u ", get_count());
                }


}
----------------------------------------------------------------------
```

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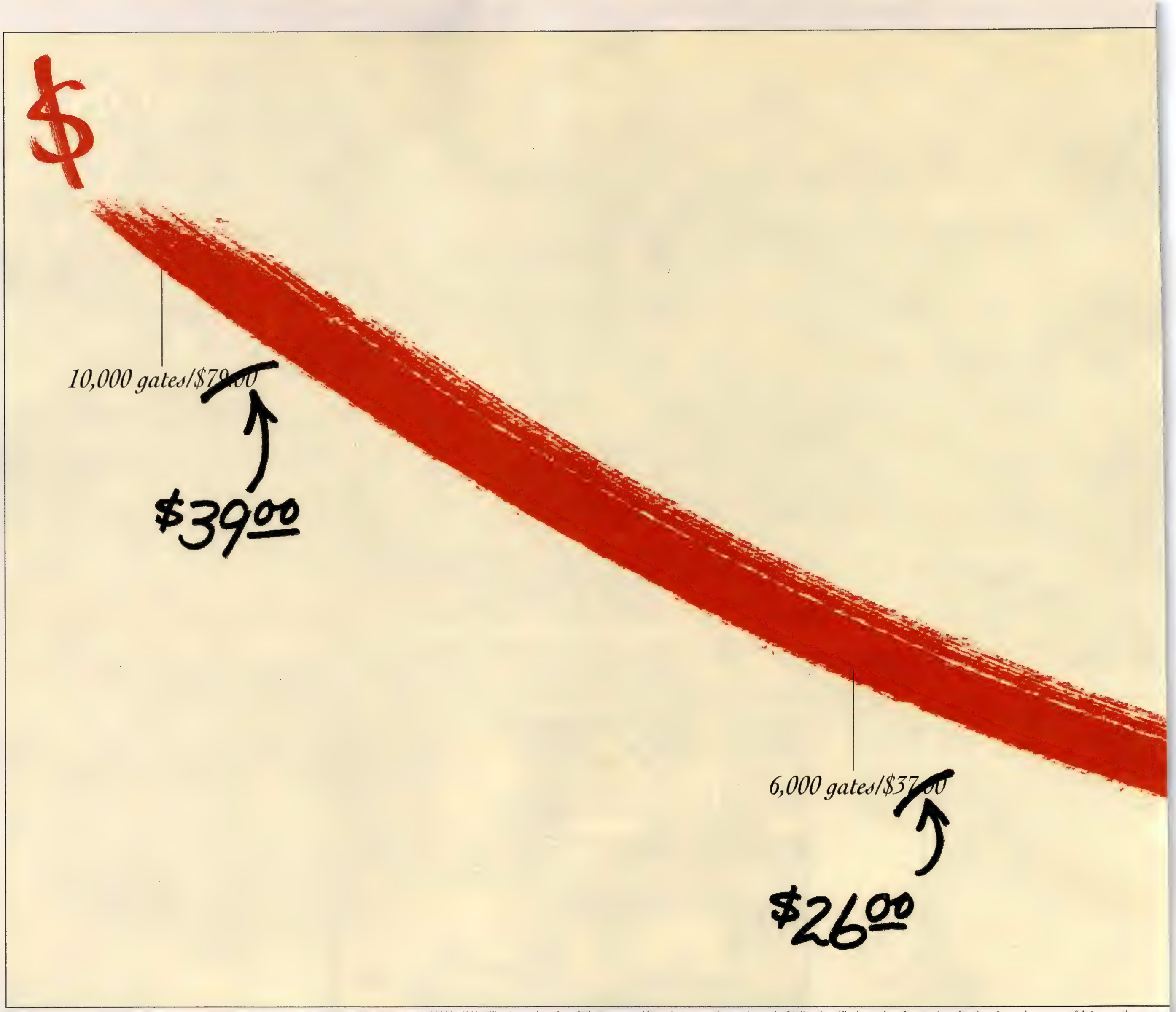

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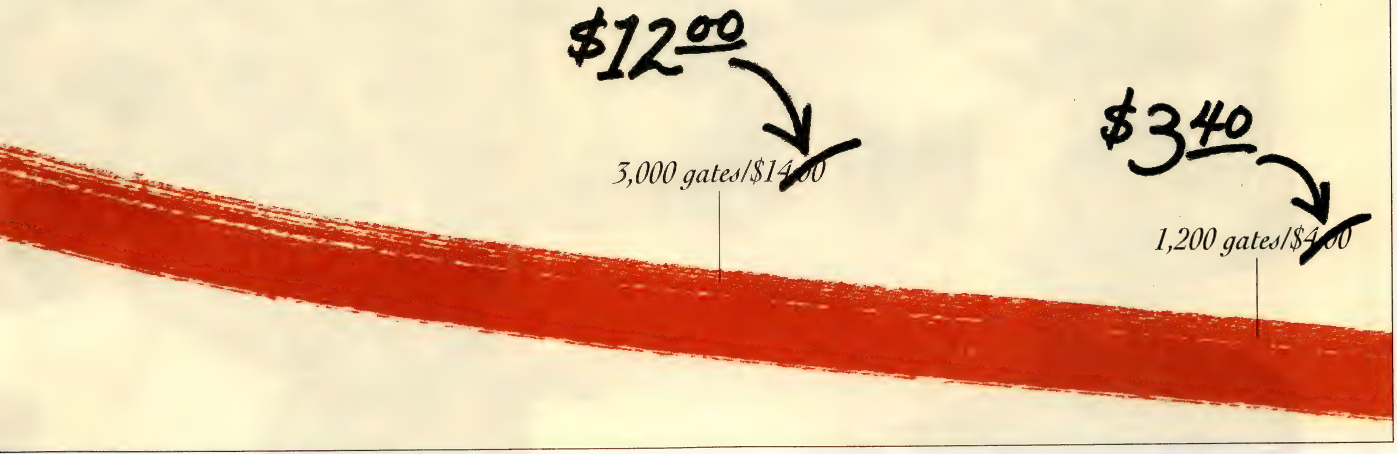

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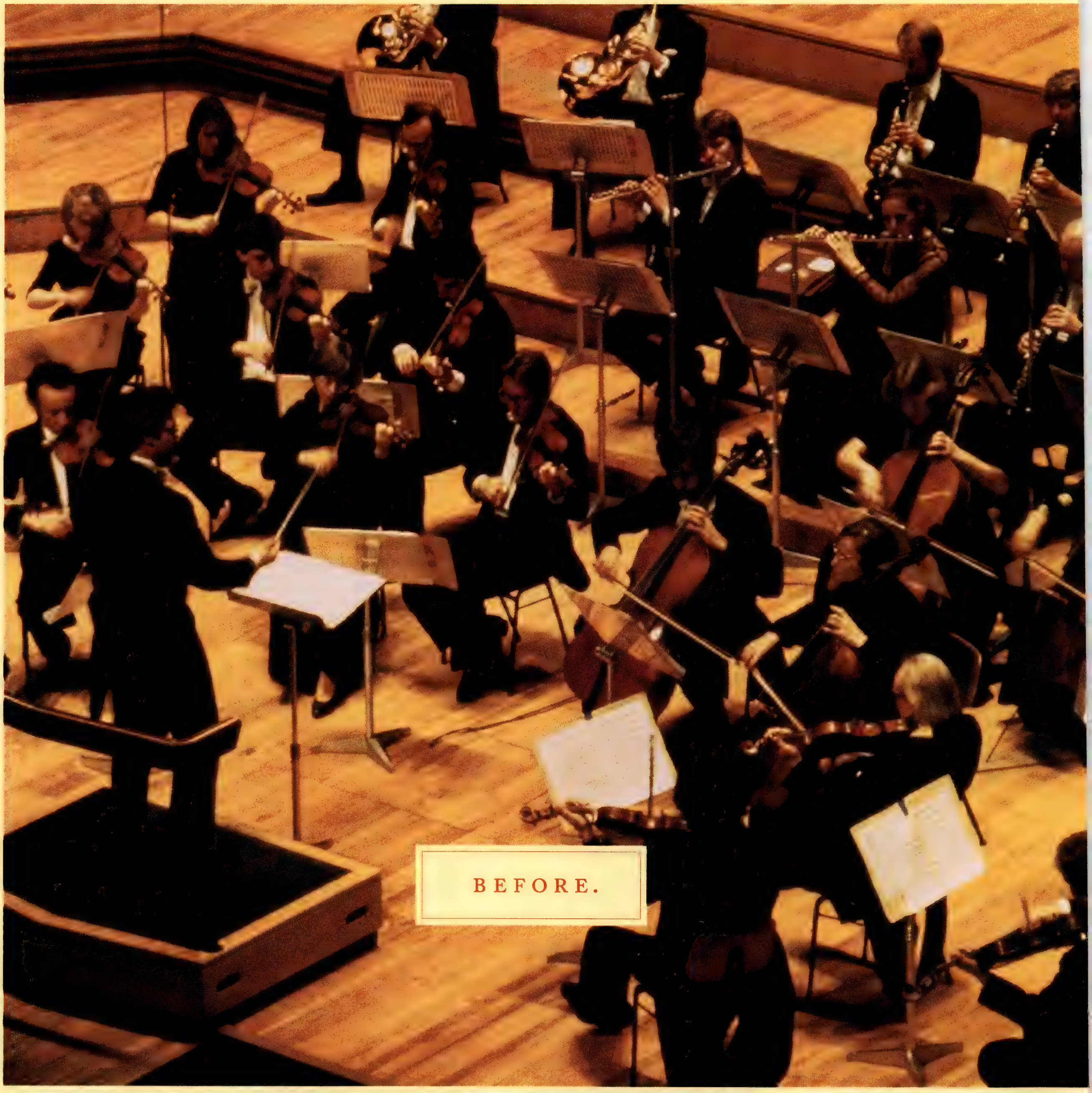

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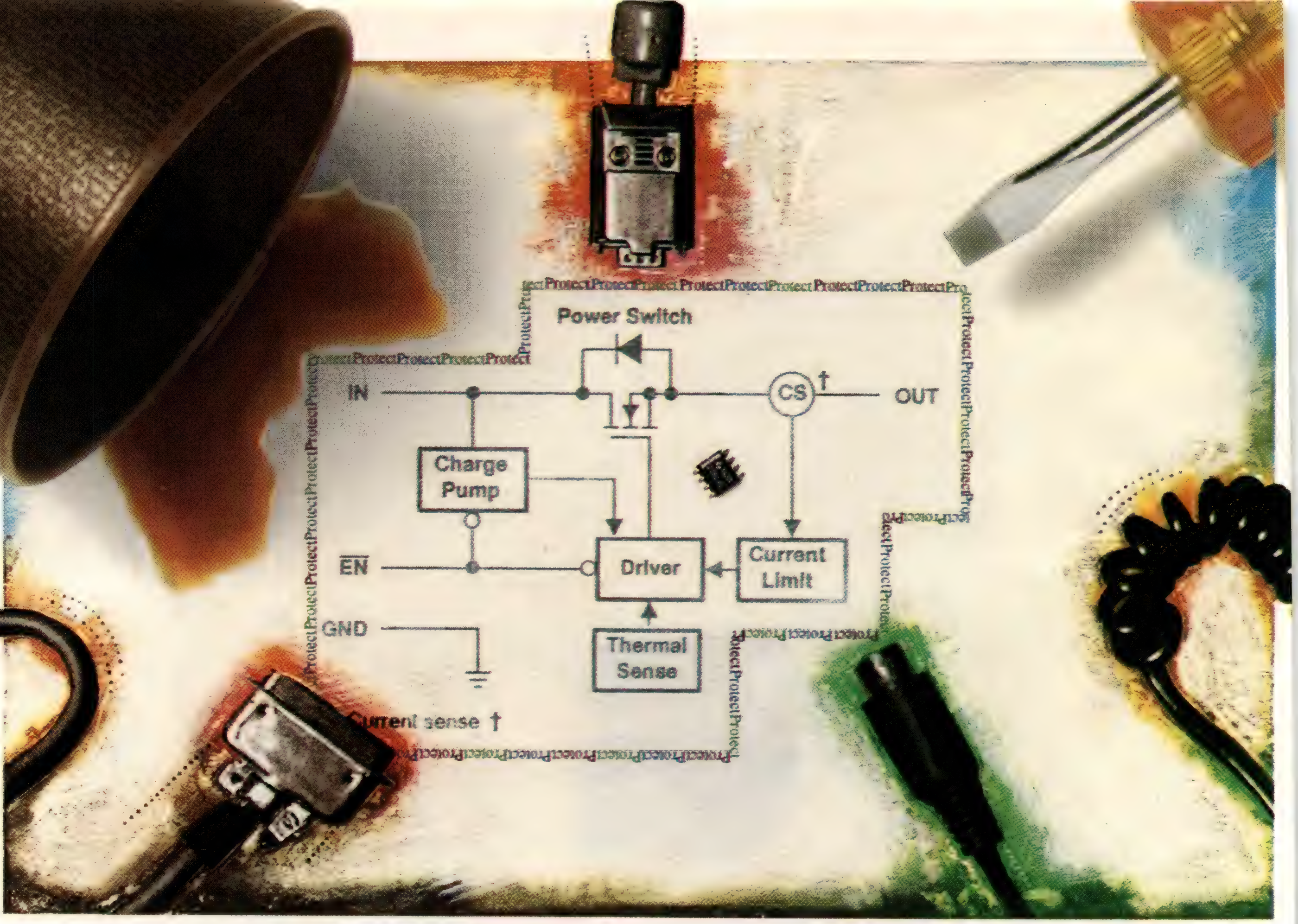

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Manufacturing, design partnership reduces PC Card assembly costs

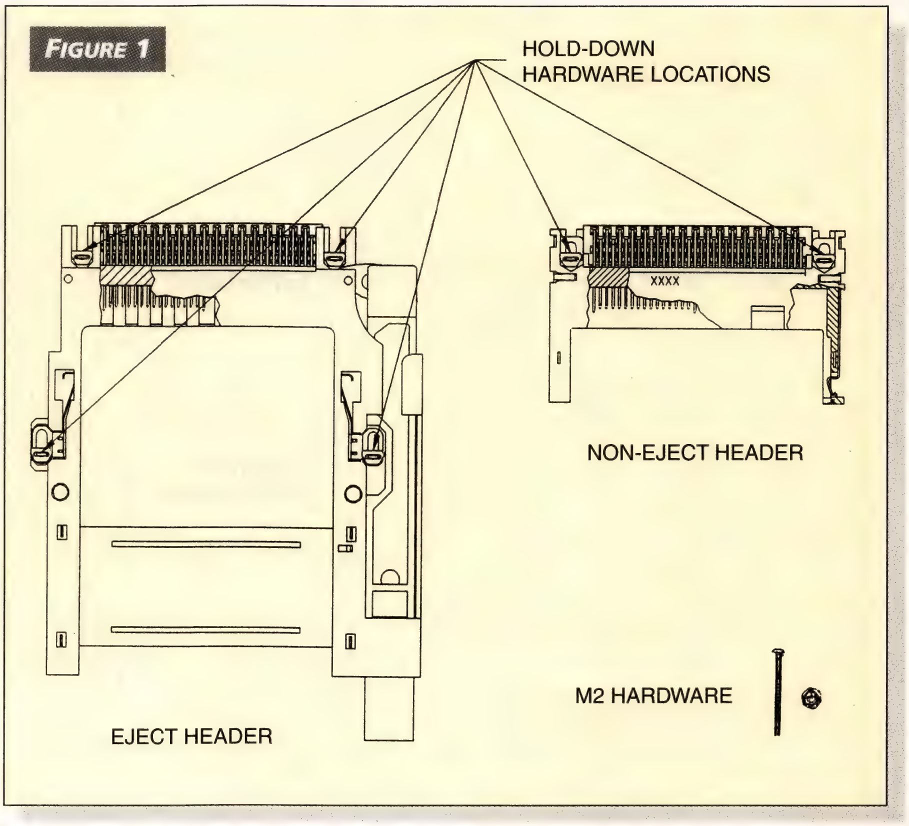
BILL KUYPERS, ROBINSON NUGENT INC

The traditional nuts-and-bolts approach to socket hold-down during reflow soldering gives way to an easier, faster method using metallic solder-retent pins.

One of the first places where OEMs requiring PCMCIA functions can look for cost reductions is in the area of connector components and their associated manufacturing costs. Unfortunately, the rousing success of the PCMCIA standard has all but eliminated the ability to reduce costs of the connector component itself. Limited capacity of the few quality suppliers and the scanty availability of one-to-one second sources are preventing price reductions.

Although capacity and second sourcing will improve, the current pricing structure is unfortunately at a point of minimum flexibility. Given this pricing scenario, the only viable cost-reduction avenue open to OEMs is in manufacturing.

FIGURE 1

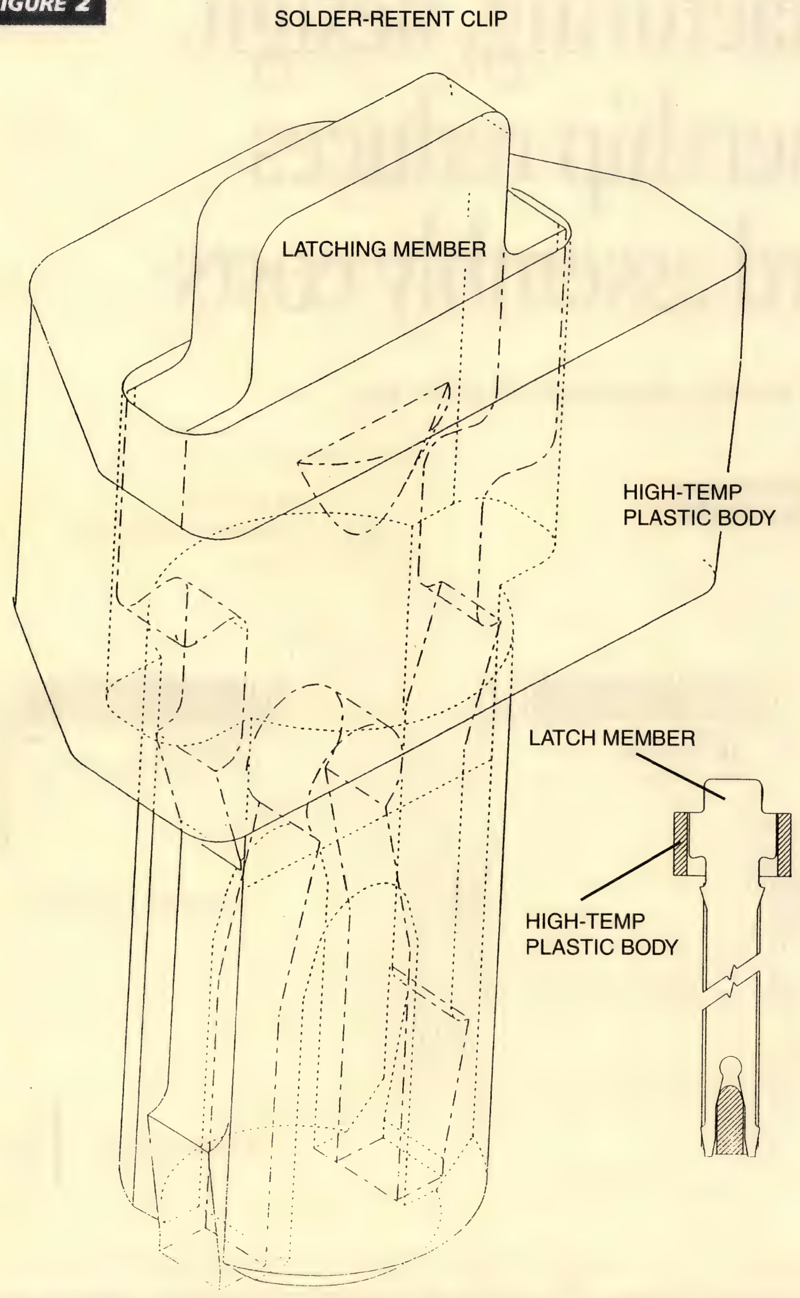


The traditional approach to holding down sockets during reflow soldering uses M2 nuts and bolts—two for non-eject sockets, four for eject sockets.

One of the principal ways to secure any connector product to a pc board is to use nuts and bolts, which provide mounting stability against board movement during soldering. They also provide a strain relief against the stress that arises in normal use. Unfortunately, because of the small hardware size and multiple hold-down locations needed for PCMCIA applications, the installation of nuts and bolts is arduous at best. Eject-type sockets require four hold-downs, and non-eject sockets typically require two.

Fig 1 shows the typical placement and hardware needed to secure sockets to the pc board. To install the necessary M2-type nuts and bolts, you must manually insert the bolt from the bottom of the board, while simultaneously providing some method to manually align the corresponding nut in the top slot of the socket. This balancing act becomes somewhat easier if you first prepare the nut with some kind of adhesive to help in securing the optimum alignment position for the corresponding bolt. What's painfully obvious is that in applications needing moderate- to high-quantity component placement, and in which automatic pick-and-place is necessary, the manual procedure all but eliminates any cost advantage the use of nuts and bolts could provide.

FIGURE 2



This solder-retent clip is a zero-insertion-force device that eliminates the need for hard-to-install nuts and bolts.

Scrapping the nuts and bolts

In the effort to facilitate automatic pick-and-place of these sockets and thereby reduce costs, several objectives are necessary to provide a viable alternative to the hand-placement procedures. First, the alternative process must be suitable for all varieties of pick-and-place equipment, from the current Fuji lines to Dynapert equipment. Because of the large variations in parameters (such as placement tolerances and pushdown forces) of these pick-and-place machines, the need exists for an inherent solder-retent clip that you can install with zero insertion force (ZIF).

This ZIF solder-retent clip (**Fig 2**) must be inherent in the sense that it must be an integral, preinstalled option on the PCMCIA socket. Preinstallation eliminates the need for costly hand insertion into the socket, and also eliminates the need to order and stock an additional part. To facilitate pick-and-place procedures, the solder-retent clip must also provide alignment to the pc board via its mounting through holes. Therefore, the solder-retent clip must extend beyond the insulator or body of the socket to provide this necessary alignment.

As you can see in **Fig 2**, the solder-retent clip is a true ZIF part, with the latching member entirely encapsulated by the high-temperature plastic body. The socket manufacturer then installs the body into the existing hold-down

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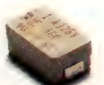
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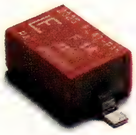
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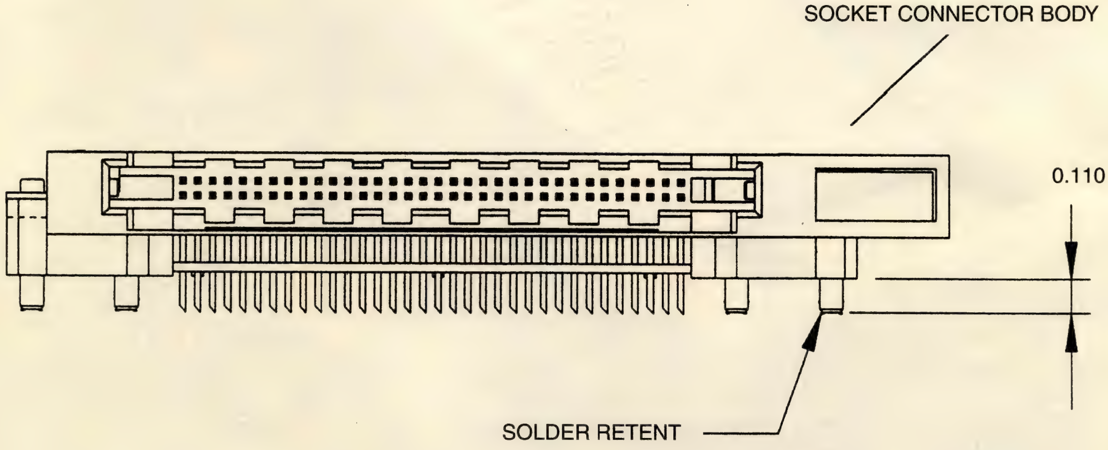
PC CARD ASSEMBLY

holes of the socket insulator, as shown in **Fig 3**. Note that the solder-retent clip extends beyond the flush body of the PCMCIA socket by 0.110 in. (on average) to provide alignment. The design and manufacturing departments at most users' facilities require the solder-retent clip to fit into existing through holes currently used for hold-down hardware on the pc boards. To accommodate this need, the solder-retent pin is designed to fit into the same 0.086-in. hole a typical M2 bolt would require.

The final aspect of the solder-retent clip to consider is the retent member itself. Based on current user applications, the retent clip must accommodate pc-board thicknesses ranging from 0.040 to 0.093 in. An additional requirement is that the clip provide a minimum hold-down force of 5 lbs, a figure deemed necessary to keep the socket stabilized during the soldering process. The solder clip must also be easy to activate without the use of special tools or hardware.

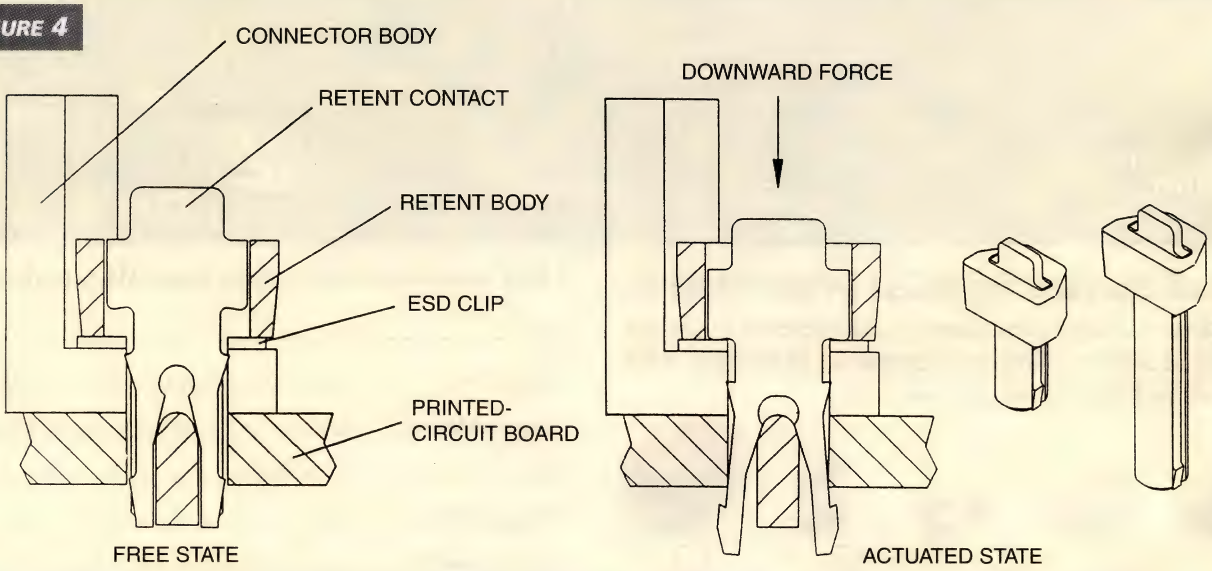
Because many applications require the use of an ESD-clip

FIGURE 3



The solder-retent clip extends beyond the flush body of the PCMCIA socket by 0.110 in. to provide alignment.

FIGURE 4



The solder-retent clip provides both a gripping action for socket retention and an electrical connection to the ESD clip.

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system (which typically carries the ground path through the mounting hardware) in the socket, the retent clip should be conductive and should make contact with the ESD clips. Finally, the retent clip should be able to adequately wick solder so that, once soldered, the clip provides a hold-down strength of at least 10 lbs. This 10-lb force is adequate to provide the necessary retention of the socket on the pc board, in order to resist any forces in the x- or y-axis during insertion and extraction of PC Cards, either into an eject or non-eject socket.

Fig 4 provides an overview of how the retent-clip system meets the cited requirements. As shown, you activate the metallic retent clip by pushing down on its head with a simple screwdriver or any other flat-tip device. This downward motion causes the inherent plastic beam of the solder-retent-clip body to spread the two independent "legs" of the solder clip. This simultaneous downward and outward motion of the retent clip's legs provides the necessary retention forces needed to stabilize the socket during the reflow process. Because the retent clip is made of stamped metal, it provides you with a solderable clip that is also conductive.

As you can see in **Fig 5**, the head of the activated retent clip rests squarely on the extension of the socket's ESD clip, and, thus, provides the needed ground path. The user's cost averages about $0.04 per solder-retent clip, or $0.16 total for an eject socket. If you compare this cost with current manufacturing direct-labor costs, the savings are at least $0.50 per socket. This conservative calculation assumes an average manufacturing labor cost of $14 per hour, or $0.23 per minute. The calculation uses an optimistic rate of 2.87 minutes to install four M2 nuts and bolts.

As the need for keeping costs down extends to all areas of consumer-electronics design and manufacturing, savings such as those achieved by using solder-retent clips become significant. In a marketplace where every cent counts, such cost savings become particularly crucial if your competitor enjoys them and you don't. EDN

Author's biography

Bill Kuypers is product-marketing manager at Robinson Nugent Inc in New Albany, IN, where he's worked for two years. He obtained BS, BA, and MBA degrees from the University of Florida, Gainesville, FL. He qualified as a CPA at Florida Atlantic University, Boca Raton, FL. Kuypers is a member of PCMCIA.

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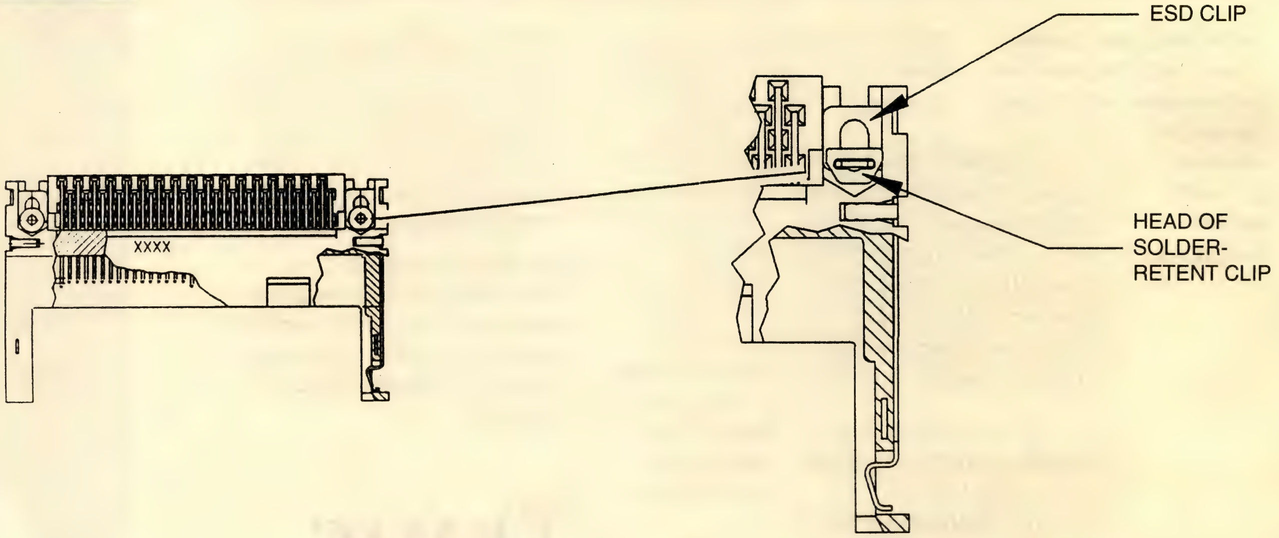
FIGURE 5



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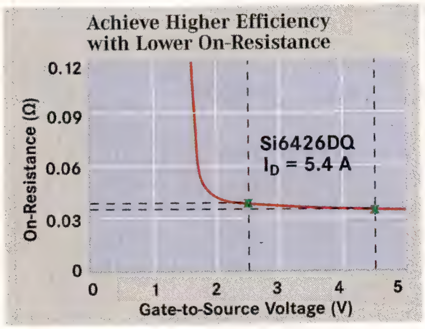

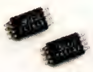

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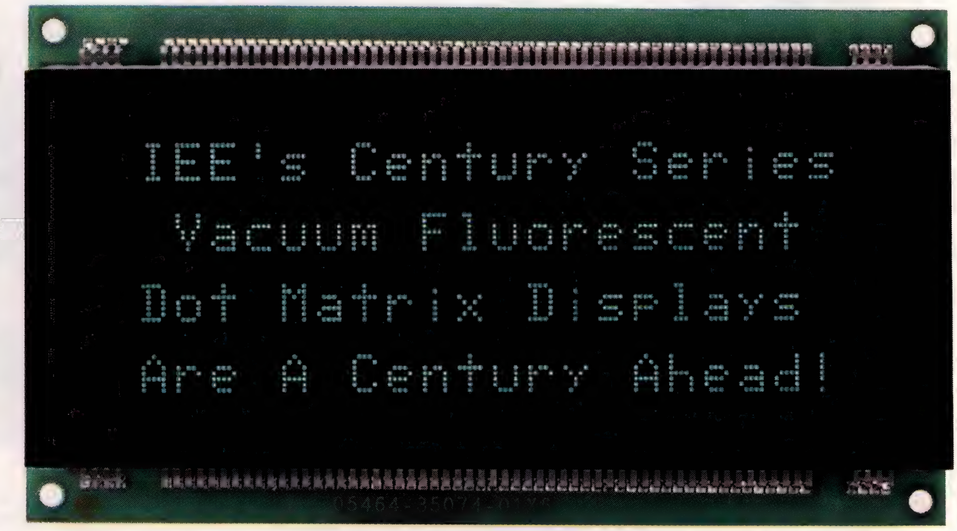

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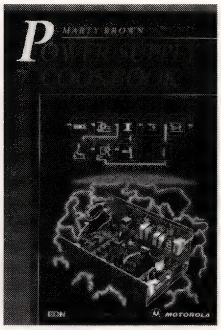

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Careful system analysis yields optimum IC-based PCMCIA power control

BOB WOLBERT, MICREL SEMICONDUCTOR

In designing power-management circuitry into a PCMCIA-standard PC Card, you face an economic trade-off between power-switch on-resistance and power-supply accuracy.

While the PCMCIA PC Card standard provides a framework for system design, it also allows considerable latitude to interpret such aspects as power management. Even the latest specification, introduced in March, requires reading between the lines to successfully design a PC Card slot into a system.

When choosing a PCMCIA power controller, consider

- Functionality: V_{CC} selection (3.3 or 5V); V_{PP} selection (12, 5, 3.3, or 0V)
- Acceptably low R_{ON}
- Protection: linear current limiting and overtemperature shutdown
- Controller interface without external components
- Error-indicator feedback to logic controller
- Controlled rise times to ensure no cross conduction or ringing.

The first item, functionality, presents you with a basic decision. Two types of systems exist today: those that have a single V_{CC} supply (generally 5V) and those with dual supplies (3.3 and 5V). If your target system uses only cards with a single V_{CC}, then you need not worry about 3.3/5V selection. However, you then need to consider the compatibility issues that can arise because your system lacks a "standard" feature. The same argument applies to the various V_{PP} voltages.

Acceptably low R_{ON} is a more difficult consideration that requires interpreting the PCMCIA specification. Protection features are important for a long service life and a good warranty record. Fumbling fingers, probing pencils, and shorted cards can destroy an unprotected slot. A "glueless" interface with the logic controller minimizes board space, complexity, and cost. An error flag feeds back slot-fault-status information that enables the logic controller to take protective action. Controlled rise times prevent damaging voltage overshoot that could destroy sensitive card electronics and prevent power-wasting "shoot through."

PCMCIA specifications

The following discussion is valid for any system, from a handheld data-acquisition system to a high-performance workstation. We'll start by examining the PCMCIA PC Card specification for V_{CC}. This supply, previously 5V only, is the main power source for the card. The new low-voltage option mandates a "cold socket" with V_{CC} disabled until you insert the card. A combination of voltage-select pins and mechanical keys on the card and socket differentiates standard (5V) and low-voltage cards. The keys prevent low-voltage cards from fitting into 5V sockets. The voltage-select pins signal which initial voltage the card accepts.

The current requirement for V_{CC} is 1A max. The specification allows systems using small batteries incapable of supplying large loads to simply reject high-current cards. The PC Card standard limits rise and fall times (measured between the 10 and 90% points), as well as transition timing.

Figs 1 and **2** show these limits. Rise time, t_1, must be between 100 µsec and 100 msec. Fall time, t_2, must be between 3 and 300 msec.

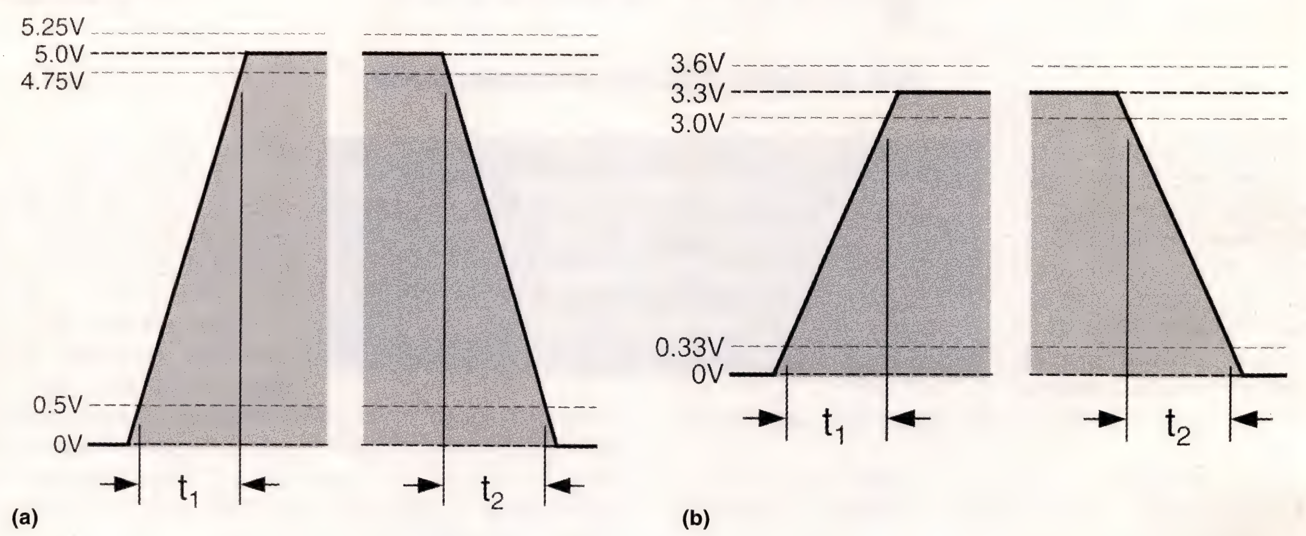
A dual-V_{CC} voltage capability creates a new problem: the need to change from one V_{CC} level to another. The timing diagram in **Fig 2** shows the sequence. Upon receipt of the command to change V_{CC}, the power-control circuit must turn off the present V_{CC} and let it drop below 0.8V. After at least 100 msec, the circuit enables the new supply voltage, following the same rise-time specification: 100 µsec to 100 msec from the 10 to 90% points.

V_{PP} requirements

The latest PC Card standard maintains the poorly defined specification for the "program and peripheral" power supply, V_{PP}, intended for flash-memory write operations. The V_{PP} voltage is generally either V_{CC} or 12V. The spec defines two independent V_{PP} pins, V_{PP1} and V_{PP2}. Many manufacturers combine these pins and drive them together. No known PC Card has a problem with this short cut, but it technically violates the specification.

Though we could justify the same amount of current for V_{PP} as for V_{CC}, 12V at 1A represents a power of 12W, which would seriously cut battery life. A more realistic approach is to evaluate the predominant V_{PP} client's requirement: the flash-memory card. Standard flash cards require 12V at a current between 30 and 120 mA for erasing and programming, to evaluate the predominate V_{PP} client's requirement: the flash-memory card. Standard flash cards require 12V at a current between 30 and 120 mA for erasing and programming, and demand 5% V_{PP} accuracy for these delicate operations. The spec does not define V_{PP} switching times. For flash cards,

FIGURE 1



V_{CC} rise time (t_1) must be between 100 µsec and 100 msec; fall time (t_2) must fall within 3 and 300 msec.

TABLE 1—V_{CC} PIN POWER-SUPPLY REQUIREMENTS

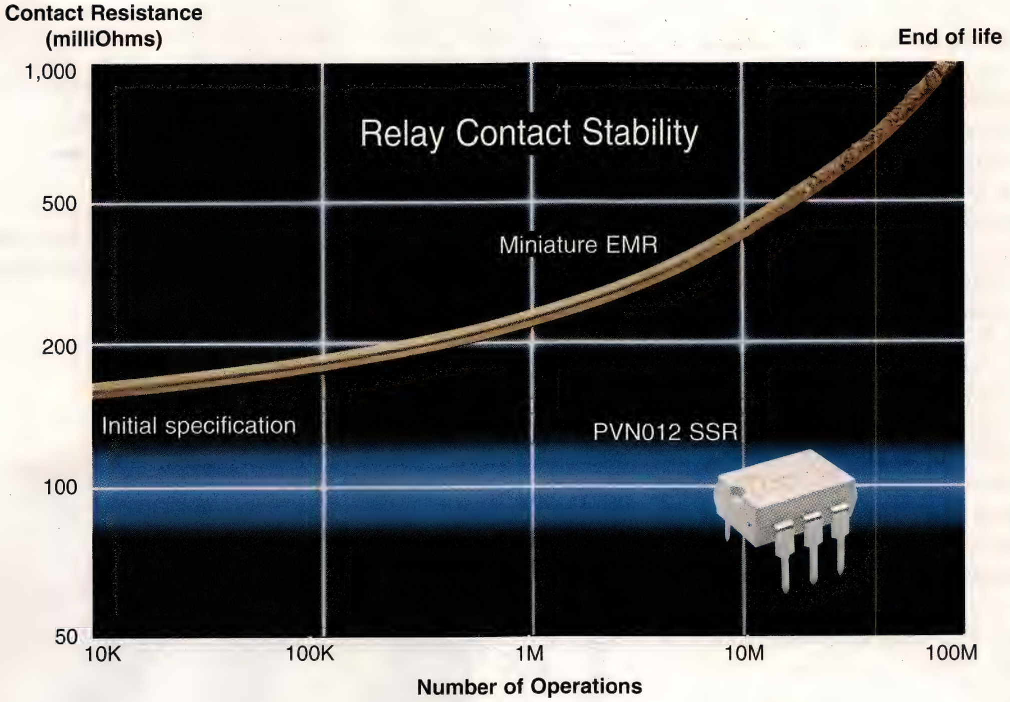
V_{CC}=5V supply accuracy (%)	±1	±2	±3	±4	±5
Maximum switch resistance (mΩ)	15	105	55	5	—
V_{CC}=3.3V supply accuracy (%)	±1	±2	±3	±4	±5
Maximum switch resistance (mΩ)	222	18	156	123	90

TABLE 2—V_{PP} PIN POWER-SUPPLY REQUIREMENTS

V_{PP}=12V supply accuracy (%)	±1	±2	±3	±4
Maximum switch resistance (mΩ) (at 120 mA)	4.7	3.5	2.3	1.1
V_{CC}=5V supply accuracy (%)	±1	±2	±3	±4
Maximum switch resistance (mΩ) (at 60 mA)	3.3	2.4	1.6	0.79

The 100mΩ relay is here to last.

Or why our new low contact resistance PVN012 solid-state relay saves you more than copper.



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Our 6-lead DIP relay switches ac or dc signals up to 20V. And handles 4.5A loads for the highest current density of any relay. Which means our solid-state relays save you more over time than copper-contact mechanicals.

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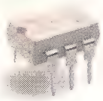
PVN012 Solid-State Relay shown actual size.



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CIRCLE NO. 161

writing is prohibited until the V_{PP} supply is stable, so supply stabilization effectively determines the write-access time of a flash "disk." However, excessively fast rise times lead to ringing that can destroy sensitive flash memories. Therefore, you should strive for maximum rise time with zero overshoot. Practical circuits perform this task in 10 to 100 msec.

PC Card slot implementation

A critical requirement for compatibility, performance, and reliability in the field is a low voltage drop at the maximum expected supply current. The V_{CC} supply, with its 1A output-current specification, requires an extremely low on-resistance, as shown in **Table 1**. This table shows the highest switch resistance that allows pin voltage to meet the required V_{MIN} at a given power-supply accuracy.

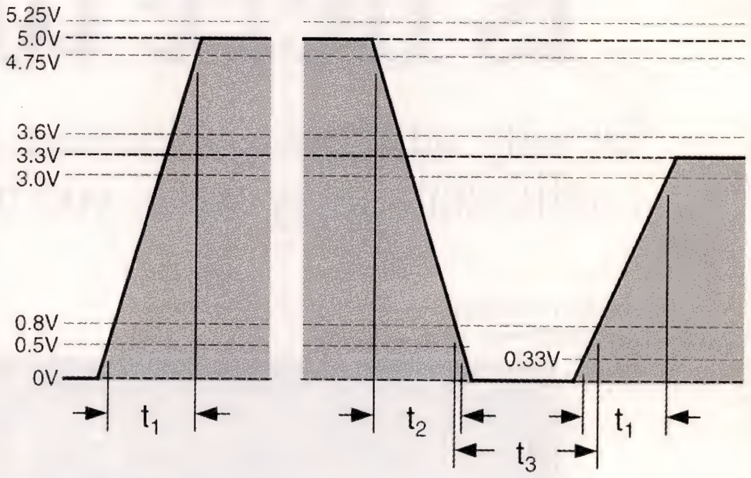
The key point to remember is that slot voltage depends on a combination of factors: input-supply accuracy, card power draw, pin resistance, and switch resistance. Reasonable values of V_{CC}=5V switch resistance and power-supply tolerance indicate that a good match exists with a ±2% V_{CC} supply and a 100-mΩ switch. The reduced accuracy requirements of the 3.3V supply allow the use of a lower cost ±5% supply with a moderate-performance 90-mΩ switch or a ±2% supply with a 190-mΩ switch. Small systems that do not support hard-disk drives or other high-current cards may accommodate higher switch resistance, thereby trading lower power-system cost for reduced compatibility.

Table 2 shows V_{PP} on-resistances. For V_{PP}=12V, acceptable switch resistance is just over 1Ω if the power system can guarantee +4% accuracy. Finite pin and pc-board trace resistances preclude the use of a ±5% supply, because the pin-voltage limit is also ±5%. When V_{PP}=V_{CC}, the current demand changes. Programmable 5V flash cards need supply currents as high as 60 mA at 5V±5%. Using the same ±2 to ±3% supply required to meet the 5V V_{CC} specification, the 5V V_{PP} on-resistance should range from 1 to 2.4Ω. No available card requires any appreciable current when V_{PP}=3.3V, so the on-resistance for this switch is not critical. Systems with V_{PP}=3.3V and 5Ω on-resistance are common, with no user complaints of incompatibility.

The R_{ON}-vs-tolerance trade-off

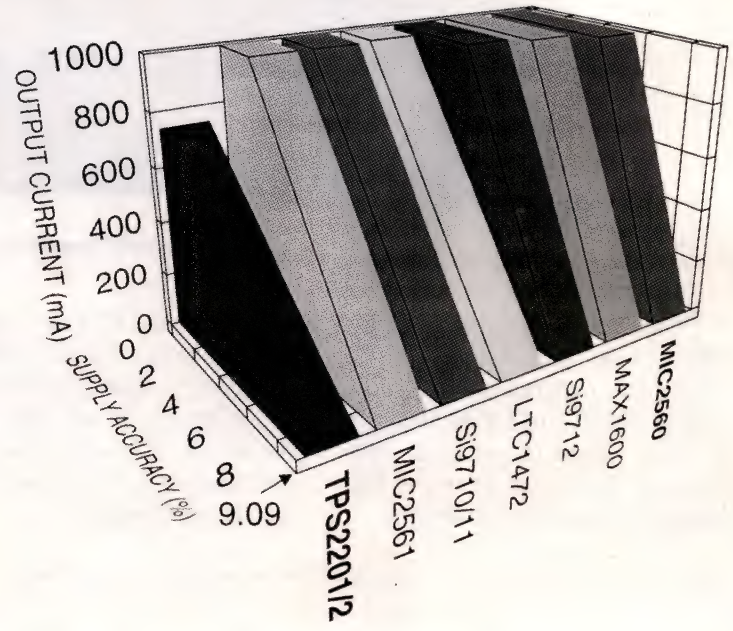
The PC Card specification provides the required pin-voltage tolerance, pin and socket

FIGURE 2



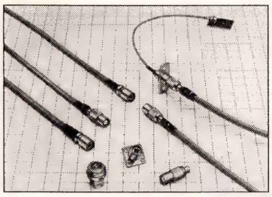
Rise and fall times for each supply in a switched 5 to 3.3V system are the same as in Fig 1. Before changing supplies, V_{CC} must go below 0.8V for at least 100 msec (t_3).

FIGURE 3



This graphic relates 3.3V power-supply accuracy and maximum output current for a number of available power switches. The size of the "safe-operating-area" blocks is a function of the switches' on-resistance.

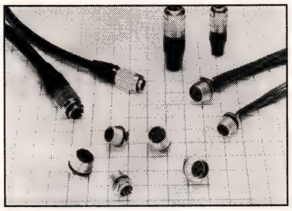
ULTRA-SMALL, PUSH-ON, LOCKING, RF COAXIAL CONNECTORS



Hirose has introduced the POD1 series of push-on, locking, RF coaxial connectors. They are about half the diameter dimension of the most popular BNC and TNC locking connectors. For instance, the diameter of jacks and plugs is as small as 7.6mm. The push-on POD-1 connectors provide optimum 50 ohm impedance for external wiring of microwave band and high-speed pulse transfer signals in mobile communications equipment. They are ideal for measuring instruments and are currently being utilized in GPS and similar RF applications. The unique push-on locking system works by locking the connector no matter which part of the connector is held. V.S.W.R is 1.3 or less from DC to 3 GHz (not including the terminator). Contact the sales department, **Hirose Electric (U.S.A.), Inc.**, 2688 Westhills Court, Simi Valley, CA 93065. (805) 522-7958 or fax (805) 522-3217. For instant fax catalog information: 1-800-879-8071. Ask for #4004.

CIRCLE NO. 185

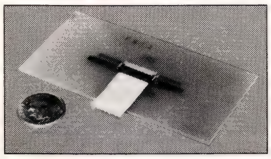
WORLD'S SMALLEST SUBMINIATURE, ROUND, MULTI-CONTACT CONNECTORS



Hirose is now providing the HR25 series of subminiature, round, multi-contact connectors. Ideal for use with miniature and high-density designs, the HR25 series offers a maximum of 20 contacts which have been condensed into an outside diameter of 12.5mm and a maximum of eight contacts into 10.5mm to achieve the world's smallest, high-density screw lock connectors. Available in a range of 4, 6, 8, 12, 16 or 20 contacts, the HR25 series is ideal for a wide range of applications, including CCD cameras, measuring instruments, sensors and interfaces for mobile radios. Contact the sales department, **Hirose Electric (U.S.A.), Inc.**, 2688 Westhills Court, Simi Valley, CA 93065 (805) 522-7958 or fax (805) 522-3217. For instant fax catalog information: 1-800-879-8071. Ask for #1007.

CIRCLE NO. 186

"FLIP-LOCK" SMT/ZIF TYPE FLEXIBLE PC BOARD CONNECTOR



Hirose Electric (U.S.A.), Inc., is producing the FH12 series of miniature connectors for FPC/FFC use. These newly developed connectors use a "flip-lock" concept and can be used with surface mount technology to prevent problems associated with slide-lock systems. FH12 series connectors have spacing of 0.5mm (0.020") and are suited to high density mounting, with a mounting height of only 2mm. The new connector has also been reduced by 1.7mm in length compared to earlier Hirose products. It is available with 10, 15, 20, 24, 30, 33, 36, 40, 45 and 50-positions. Hirose's one-touch ZIF (zero insertion force) technology offers labor-savings, even with multiple contacts. Contact **Hirose Electric (U.S.A.), Inc.**, 2688 Westhills Court, Simi Valley, CA 93065-6235. (805) 522-7958 or fax (805) 522-3217. For instant fax catalog information: 1-800-879-8071, ask for #6004.

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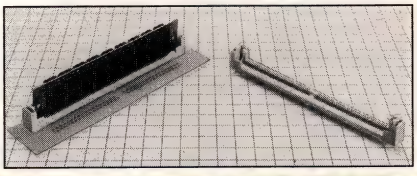
72-pin SIMM SOCKET

Hirose is providing the SX3, a newly developed SIMM socket suitable for JEDEC standard 72-pin memory module boards with 1.27mm (0.050") spacing. Through the use of FEM analysis, Hirose has molded a latch system which is more durable and cost-effective than other products on the market. Contacts on the SX3 provide high performance by utilizing a smooth, rolled-surface design. Preloaded contacts provide a stable, reliable force and make the SX3 ideal for personal computers, workstations, computer peripherals, hard disks, office automation equipment and measuring instruments. For further information, contact the sales department, **Hirose Electric (U.S.A.), Inc.**, 2688 Westhills Court, Simi Valley, CA 93065. (805) 522-7958 or fax (805) 522-3217. For instant fax catalog information: 1-800-879-8071. Ask for #5023.



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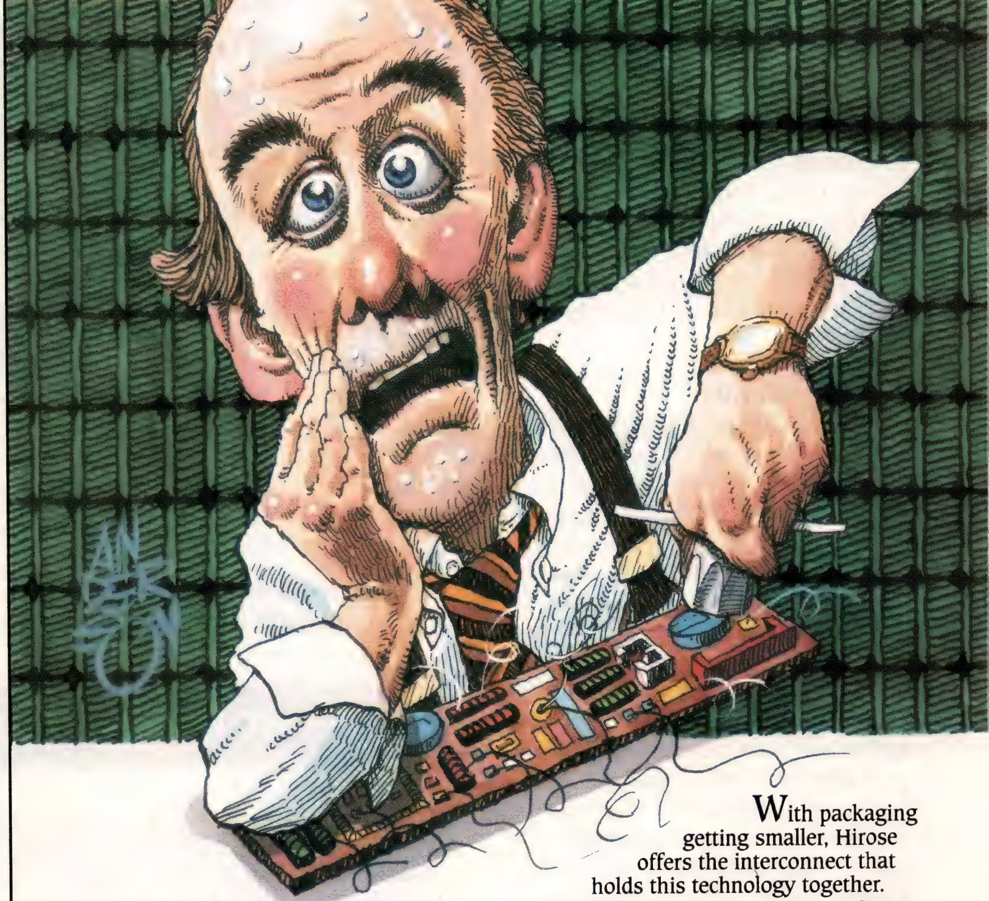

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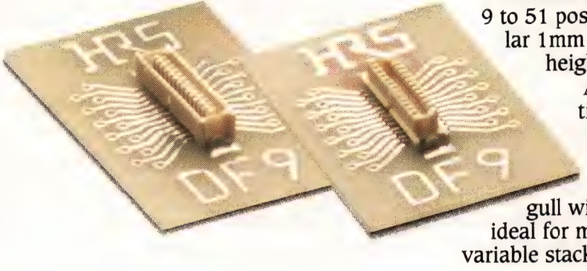
It is Hirose's growing series of low-cost, high-density, board-to-board SMT stacking connectors.

For starters, the new DF15 has tight 0.65mm (0.026") spacing and from 20 to 50 contacts, with stacking heights from 4mm to 8mm in 1mm steps.

Another board-to-board connector, with 9 to 51 positions, is the DF9. It has a popular 1mm (0.39") center line and a mated height between PCBs of 4.3mm.

Available in 20 to 60 positions, Hirose's DF12 offers the tightest spacing with its 0.5mm (0.020") center line.

Choose from a large family of gull wing contact connectors, each ideal for miniaturization. Hirose offers variable stacking heights and a variety of contact centers. Plus, tape and reel packaging for pick and place automation to reduce production costs.



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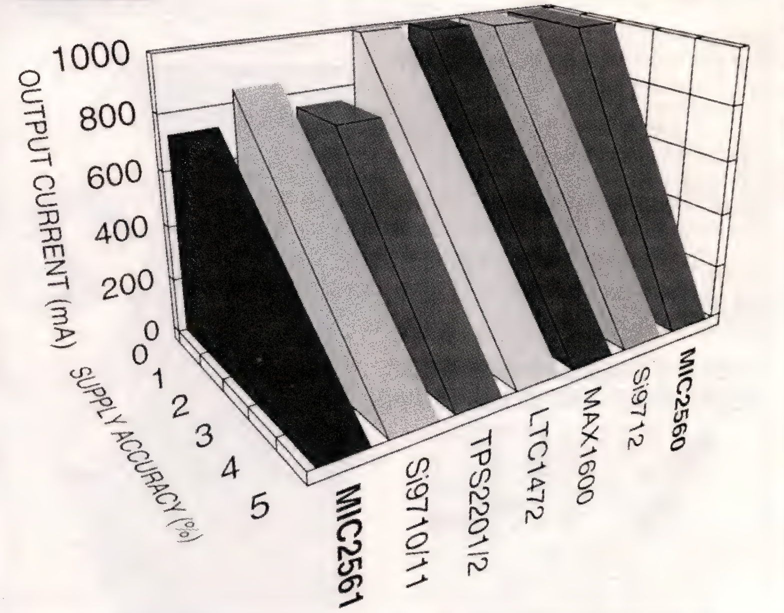
CIRCLE NO. 189

resistance, and the maximum allowable current. Using these numbers, you can determine the maximum allowable power-switch on-resistance and power-supply tolerance. Note that, in many cases, a standard ±5% supply is inadequate to meet the specifications. A more expensive, tighter tolerance supply is necessary, and the tolerance requirement becomes more stringent when you use switches with higher on-resistance. Generally, you can avoid the higher cost of a high-precision power supply by using a slightly more expensive, lower-resistance switch. In general, a power supply with a ±2% tolerance is about \$2 per output more expensive than a ±5% supply. This cost increases rapidly when you require even tighter tolerances.

FIGURE 4



Because of excessive on-resistance, some available power switches are unsuitable for 5V, 1A applications.

Design examples

Consider three specific system applications with differing power requirements. Proper electronic design requires taking account of the expected worst-case conditions, so we'll assume a 70°C die temperature for the switch. It's not wise to use room-temperature specifications for portable systems.

The first example involves a subnotebook computer. A user considers such a computer, equipped with a 486 or better processor, as a full-featured machine. Expectations are that the computer will support *any* PC Card, including modems and hard-disk drives. Therefore, the machine must provide the full 1A V_{CC} output capability. Here, we choose a Micrel Semiconductor MIC2560 V_{CC} and V_{PP} power controller for switching. Using the on-resistance specs in **Table 3**, let's examine the requirements for the power-supply specifications:

TABLE 3—REPRESENTATIVE PC CARD POWER SWITCHES

	V_{CC} switch V (lower is better)		V_{PP} switch V (lower is better)			Supply tolerance (%) (wider is better) @1A		@750 mA	
Device	**3.3V**	**5V**	**3.3V**	**5V**	**12V**	**3.3V**	**5V**	**3.3V**	**5V**
MIC2560	0.066	0.100	3	1	1	5.7	2.1	6.6	2.8
MIC2561	0.185	0.300	3	1	1	2.1	—	3.9	—
LTC1472	0.192	0.192	6	6	1.2	1.9	0.26	3.7	1.4
MAX1600	0.096	0.168	3	3	1.2	2.6	0.74	4.3	1.8
Si9711	0.185	0.250	0.5	0.6	0.2	2.1	—	3.9	0.58
Si9712	0.114	0.150	0.4	0.4	0.2	4.3	1.1	5.5	2.1
TPS2201	0.360	0.192	7.2	7.2	1.2	—	—	—	1.4

V_{CC}=5V, I_{OUT}=1A
MIC2560 on-resistance=100 mΩ
Socket pin resistance=+45 mΩ
Total resistance=145 mΩ.

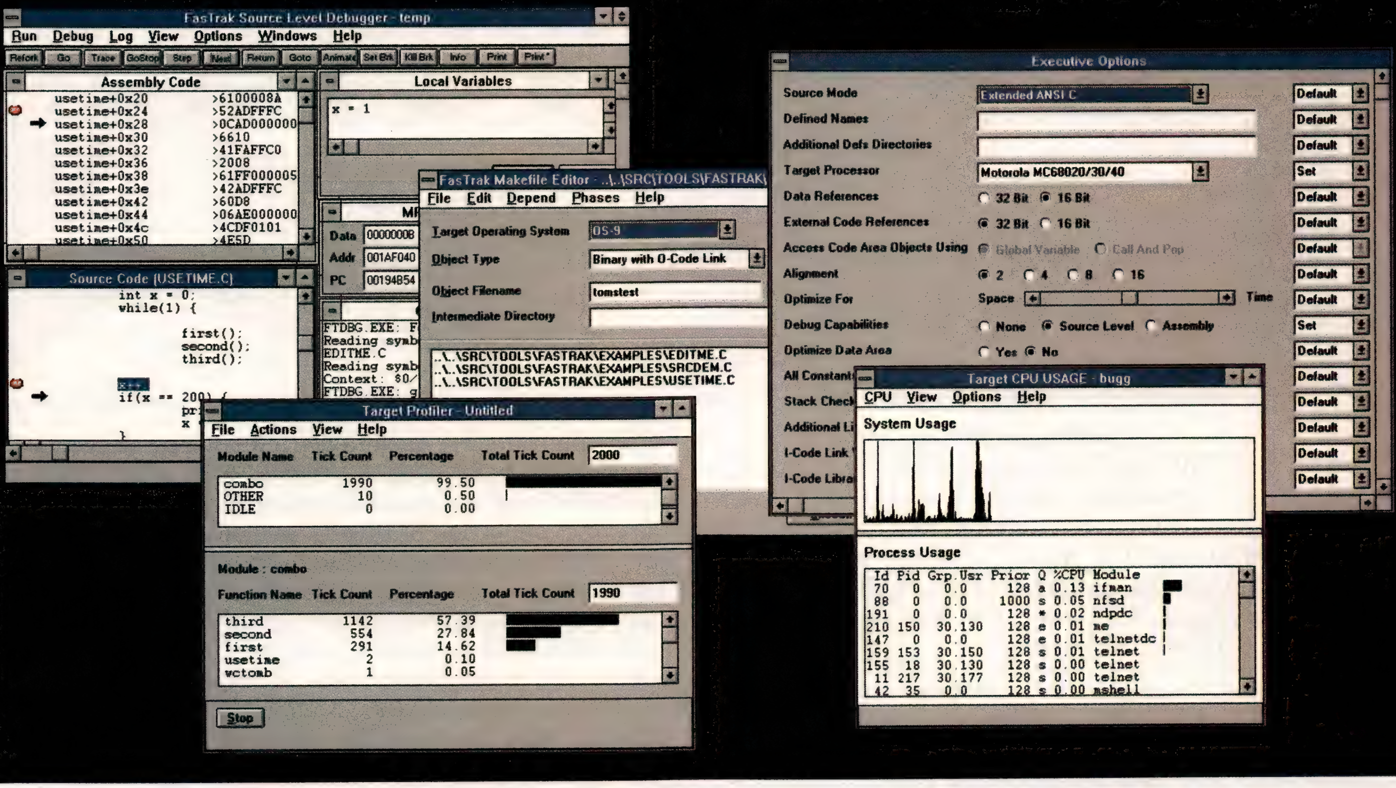
So the minimum V_{CC} input for 4.75V at the card is 4.75+(1A×145 mΩ)=4.895V. The system power supply must provide 4.895 to 5.25V. You could state this as 5V+5%, –2.1%, or 5.073V±3.5%. This 5.073V nominal supply voltage is well within the acceptable tolerance of a standard 5V±5% supply, so it can power all the 5V components in the system.

V_{CC}=3.3V, I_{OUT}=1A
MIC2560 on-resistance=66 mΩ
Socket pin resistance=+45 mΩ
Total resistance=111 mΩ.

The minimum V_{CC} input for 3.0V at the card is 3.0V+(1A×111 mΩ)=3.111V. The required power-supply voltage is from 3.111 to 3.6V. A 3.3V+9%, –5.7%, or a 3.356V±7.3% supply is suitable.

In the second example, we consider a handheld, or palmtop, computer. These machines generally require a communications capability via a PC Card modem. They usually don't accommodate a hard-disk drive because of battery-capacity constraints. Assuming a modem draws 300 mA from a 5 or 3.3V supply, we select the MIC2561 V_{CC} and V_{PP} power controller. The palmtop's supply requirements are:

Your Window to OS-9 Real-Time Development


FasTrak Source Level Debugger - temp
Run Debug Log View Options Windows Help
Refork Go Trace GoStop Step Next Return Goto Animate Set Brk Kill Brk Info Print Print*
Assembly Code
Local Variables
Source Code (USETIME.C)
MP
FasTrak Makefile Editor - ..\..\SRC\TOOLS\FASTRAK\
File Edit Depend Phases Help
Executive Options
Target CPU USAGE - bugg
CPU View Options Help
System Usage
Process Usage
Target Profiler - Untitled
File Actions View Help
Stop

```
usetime+0x20        >6100008A
usetime+0x24        >52ADFFFC
usetime+0x28        >0CAD000000
usetime+0x30        >6610
usetime+0x32        >41FAFFC0
usetime+0x36        >2008
usetime+0x38        >61FF000005
usetime+0x3e        >42ADFFFC
usetime+0x42        >60D8
usetime+0x44        >06AE000000
usetime+0x4c        >4CDF0101
usetime+0x50        >4E5D
```

```
x = 1
```

```
      int x = 0;
      while(1) {

              first();
              second();
              third();


      x++;
      if(x == 200) {
      pr
      x
    }
```

Data 00000008
Addr 001AF040
PC 00194B54

```
FTDBG.EXE: F
Reading symb
EDITME.C
Reading symb
Context: $0/
FTDBG.EXE: g
```

Target Operating System: OS-9
Object Type: Binary with O-Code Link
Object Filename: tomstest
Intermediate Directory:

```
..\..\SRC\TOOLS\FASTRAK\EXAMPLES\EDITME.C
..\..\SRC\TOOLS\FASTRAK\EXAMPLES\SRCDEM.C
..\..\SRC\TOOLS\FASTRAK\EXAMPLES\USETIME.C
```

Source Mode: Extended ANSI C — Default
Defined Names: — Default
Additional Defs Directories: — Default
Target Processor: Motorola MC68020/30/40 — Set
Data References: ○ 32 Bit ● 16 Bit — Default
External Code References: ● 32 Bit ○ 16 Bit — Default
Access Code Area Objects Using: ● Global Variable ○ Call And Pop — Default
Alignment: ● 2 ○ 4 ○ 8 ○ 16 — Default
Optimize For: Space … Time — Default
Debug Capabilities: ○ None ● Source Level ○ Assembly — Set
Optimize Data Area: ○ Yes ● No — Default
All Constant — Default
Stack Check — Default
Additional Li — Default
I-Code Link — Default
I-Code Libra — Default

```
 Id Pid Grp.Usr Prior Q %CPU Module
 70   0    0.0    128 a 0.13 ifman
 88   0    0.0   1000 s 0.05 nfsd
191   0    0.0    128 * 0.02 ndpdc
210 150 30.130    128 e 0.01 me
147   0    0.0    128 e 0.01 telnetdc
159 153 30.150    128 s 0.01 telnet
155  18 30.130    128 s 0.00 telnet
 11 217 30.177    128 s 0.00 telnet
 42  35    0.0    128 s 0.00 mshell
```

Module Name / Tick Count / Percentage — Total Tick Count: 2000

```
combo        1990      99.50
OTHER          10       0.50
IDLE            0       0.00
```

Module : combo

Function Name / Tick Count / Percentage — Total Tick Count: 1990

```
third        1142      57.39
second        554      27.84
first         291      14.62
usetime         2       0.10
wctomb          1       0.05
```

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CIRCLE NO. 162

TABLE 4—FEATURES OF REPRESENTATIVE POWER SWITCHES

Device	CardBus compatible	Current limiting (V_{CC})	Current limiting (V_{PP})	Over-temperature shutdown	Error flag	Logic compatible with: Cirrus	Intel	Vadem	Databook
MIC2560	✓	✓	✓	✓	✓	✓	✓	✓	✓
MIC2561	✓	✓	✓	✓	✓	✓	✓	✓	✓
LTC1472		✓	✓	✓	✓	✓	✓	✓	
MAX1600	✓	✓	✓	✓	✓	✓	✓	✓	✓
Si9711						✓	✓	✓	
Si9712	✓					✓	✓	✓	
TPS2201		✓	✓	✓	✓	✓	✓	✓	

V_{CC}=5V, I_{OUT}=300 mA
MIC2561 on-resistance=300 mΩ
Socket pin resistance=+45 mΩ
Total resistance=345 mΩ.

The minimum V_{CC} input for 4.75V at the card is 4.75V+(300 mA×345 mΩ)=4.835V. The system power supply must provide 4.835 to 5.25V. You can state this as 5V+5%, –3.4% or 5.043V±4.0%.

V_{CC}=3.3V, I_{OUT}=300 mA
MIC2561 on-resistance=185 mΩ
Socket pin resistance=+45 mΩ
Total resistance=230 mΩ.

The minimum V_{CC} input is 3.111V, which denotes a 3.3V+9%, –5.7% or a 3.356V±7.3% supply. For V_{CC}, we note that the on-resistances of the MIC2561 are suitable for the intended PC Card load, given 5V±3.4% and 3.3V±5.7% supplies. On the other hand, the MIC2560 would do the same job with 5V±4.1% and 3.3V±8% supplies. You must weigh the additional cost of the MIC2560 against the (usually much larger) added cost of a more accurate supply.

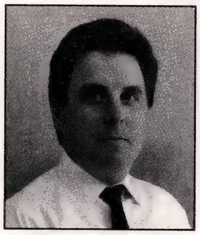
In the third example, we consider equipment used for data-taking, such as handheld loggers, DVMs, and inventory checkers. This type of equipment does not require extensive compatibility with various types of PC Cards. The equipment generally uses either SRAM or flash-memory cards and operates with a single V_{CC} voltage. If this V_{CC} is 5V, the PCMCIA specification allows hard-wiring the supply to the pin. Otherwise, a simple, single-pole MOSFET switch can enable V_{CC} to the card.

You can achieve V_{PP} control by using the MIC2557 power controller for systems that tie V_{PP1} and V_{PP2} together or the MIC2558 to support separate V_{PP} pins. Some 5V-only flash cards draw as much as 60 mA from V_{PP}. You can accommodate these cards by connecting the two halves of the MIC2558 in parallel and using a 5V+5%, –3.4% (or 5.04V±4.1%) supply. The MIC2559 has improved V_{CC}=V_{PP} on-resistance and allows the use of a 5V+5%, –4% (or 5.025V±4.4%) supply.

When selecting a power controller for PC Card slots, remember that both specified and nonspecified parameters affect compatibility. A controller must switch all required supply voltages for both V_{CC} and V_{PP} with acceptable on-resistance across the operating-temperature range and without cross conduction or ringing. It should also protect the rest of the system from any fault condition and signal the logic controller when such a fault exists. **Table 4** lists the features available in several PC Card power switches.

The switches you use for V_{CC} selection must provide a few features not mentioned in the PCMCIA specification. They must properly sequence the 3.3 and 5V supplies so no shoot-through paths exist, and they must exhibit minimal damaging voltage ringing. A price/performance trade-off exists between switch on-resistance and the required V_{CC} supply accuracy. For any given output current, the switch with lower on-resistance allows use of a lower cost, lower accuracy supply. In many cases, you realize the lowest system cost by using the best available power switch.

Author's biography



Bob Wolbert is manager of intelligent power products at Micrel Semiconductor (San Jose, CA), where he has worked for five years. His duties include applications engineering, including new-product definition. Holder of a BS in electrical and computer engineering from the University of California at Santa Barbara, Bob is a member of PCMCIA. He enjoys amateur radio—a hobby he's practiced since age 12.

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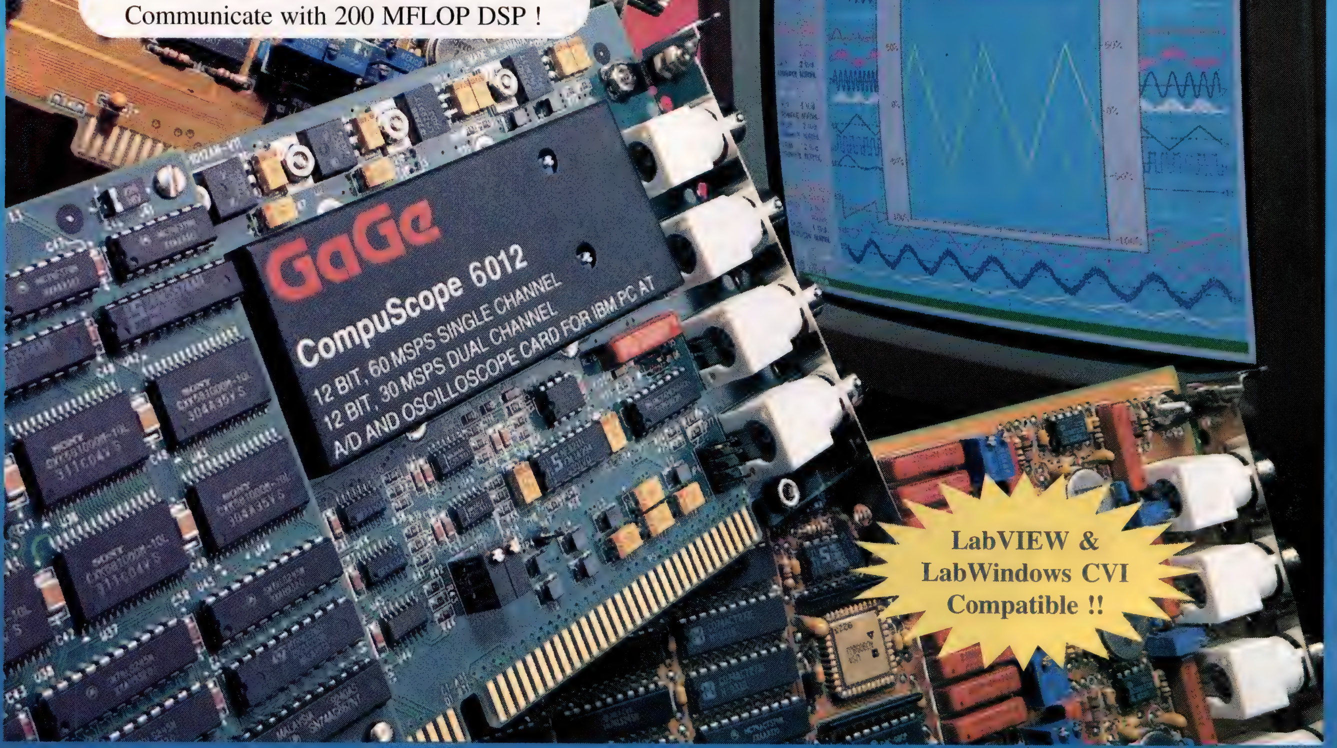
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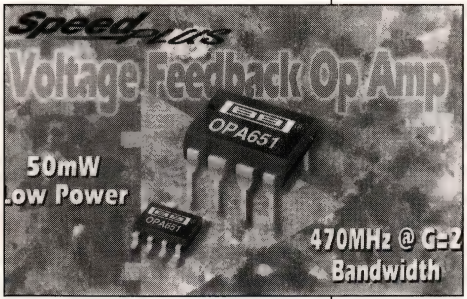
Step-up switching-regulator families offer low quiescent currents. The TC17 family of PWM step-up switching regulators has a 30-µA quiescent current. The TC18 family of pulse-frequency-modulated step-up switching regulators has a 6-µA quiescent current. Both regulators are available with standard output voltages of 5, 3, and 3.3V. Custom output voltages of 2.7 to 7.5V in 0.1V steps are also available. Output voltages are accurate to ±2.5%. The regulators come in SOT-89 packages and suit use in small, portable equipment, such as pagers and cellular phones. $1.66 (1000). **Telcom Semiconductor Inc**, Mountain View, CA. (415) 968-9241. **Circle No. 400**

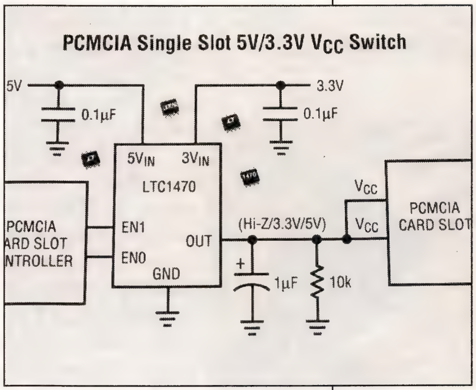


▲Voltage-feedback op amp has 940-MHz gain-bandwidth product and 50-mW power dissipation. The OPA651 is compensated for stability in gains of two or greater. Key specifications include a 4-µA input-bias current, –78-dB harmonics at 5 MHz, 0.01% differential gain error, and 0.025° differential phase error. The device is available in eight-pin DIP and SO-8 packages and has performance specified from –40 to +85°C. $1.95 (1000). **Burr-Brown Corp**, Tucson, AZ. (602) 746-1111. **Circle No. 401**

High-precision voltage references offer low noise and low drift. The VRE300 series voltage references use a zener reference and a patented temperature-compensation technique. The devices are available in performance grades of 0.6-, 1-, and 2-ppm/°C TCs and 0.5-, 0.8-, and 1-mV initial error. Output voltages include 10, 5, 4.5, and 2.5V. The devices come in eight-pin DIP and surface-mount packages. From $5.80 (1000). **Thaler Corp**, Tucson, AZ. (520) 882-4000. **Circle No. 402**

Multiple-output clock synthesizer suits PCI bus systems using a Pentium processor. The W48C60-402 provides four skew-controlled CPU clock outputs, six skew-controlled PCI clock outputs, one 24-MHz clock for floppy-disk drives, one 12-MHz keyboard clock, and two 14.318-MHz reference clocks. Skew between outputs in the CPU and PCI clock-output group is 100 psec typ, jitter is ±250 psec max. The chip also has a built-in crystal oscillator circuit. It comes in a 28-pin SOIC and operates from a 3.3 or 5V source. The chip costs $2.87 (10,000). **IC Works Inc**, San Jose, CA. (408) 922-0202. **Circle No. 403**

Core-logic chip set for AMD K5, Cyrix M1, and Intel Pentium processors. The chip set includes the M1511 memory cache buffer controller, the M1513 SIO controller, and two M1512 data buffers. The chip set works with up to 150-MHz Pentium processors. It supports caches up to 1 Mbyte using pipelined-burst, burst, and standard SRAMs. Standard memory can include up to 768 Mbytes using high-performance, extended-data-out or standard DRAM. The chip set also integrates bus-mastered IDE and keyboard controllers to reduce parts count on the system board. The M1511 and M1513 come in 208-pin PQFPs, and the M1512s come in 100-pin PQFPs. The chip set costs $22 (OEM). **Acer Laboratories Inc, Pacific Technology Group**, Santa Clara, CA. (408) 764-0644. **Circle No. 404**

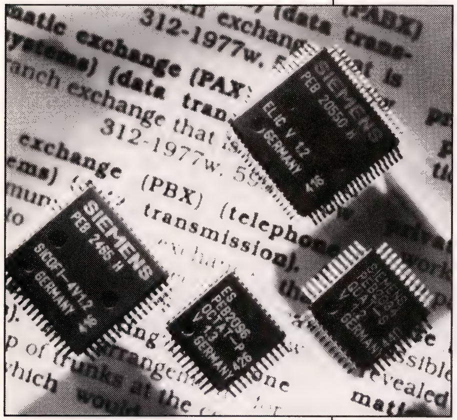


▲Power-matrix switch for PCMCIA has short-circuit protection. The LTC1470 switches among 5 and 3.3V and off. It has a 1A output-current capability and a current limit and thermal shutdown to protect the socket, the card, and the power supplies against short circuits. The 5 and 3.3V switches have typical on-resistances of 0.14 and 0.12Ω, respectively. Output leakage is 0.01 µA in the off state. A 5V supply powers the switch, which comes in an eight-lead SOIC and costs $2.35 (1000). The LTC1471 is a power switch for dual-PCMCIA-slot applications. It comes in a 16-lead SOIC and costs $3.95 (1000). **Linear Technology Corp**, Milpitas, CA. (408) 432-1900. **Circle No. 405**

10BaseT Ethernet IC supports Plug and Play ISA standard version 1.0a. The 78Q8377 stores and reads configuration information in an external serial EEPROM, avoiding the need for jumpers. The EEPROM can also contain the address of an external boot device, allowing diskless workstation boot-up. The IC includes a full-duplex Ethernet media-access controller, a 10-Mbps Manchester encoder/decoder, a 10BaseT transceiver, and an attachment-unit interface for connection to other external transceivers. The device comes in a 128-pin QFP and operates from a 5V supply. Samples are available now, and production is scheduled for the third quarter of 1995. $15.50 (1000). **Silicon Systems**, Tustin, CA. (714) 573-6200. **Circle No. 406**

ISDN user-interface chip supports Layer 1 and 2. The YM7450B basic-rate interface controller for integrated-services digital network (ISDN) has an analog driver and receiver that reduces peripherals costs; support for automatic/nonautomatic assignment of terminal endpoint identifiers; and support for European Telecommunications Standards Institute standards for European applications. The device has a power-down mode for low-power applications and comes in an 80-pin QFP or a 100-pin TQFP. Samples cost $25. An evaluation board for developing Layer 3 application software costs $395. **Yamaha Systems Technology Division**, San Jose, CA. (408) 467-2300. **Circle No. 407**

Ethernet controller has PCMCIA interface and on-chip RAM. The SMC91C94 Ethernet controller includes 4608 bytes of on-chip RAM. It also can send information over the network or to the CPU's system RAM before the controller receives a complete packet. According to the company, the feature improves performance up to 45%. Except for the addition of a PCMCIA interface, the architecture and features of the chip are the same as those of the SMC91C92. It is pin- and register-set-compatible with the earlier device. The device comes in a 100-pin QFP or TQFP and costs $15 (1000). **Standard Microsystems Corp**, Hauppauge, NY. (516) 273- 3100.
Circle No. 408



▲ICs for digital communication systems reduce chip count. The devices suit use in PBXs, key systems, voice-response units, and automatic call-distribution systems. The PEB 20550H extended line-card controller handles 32 digital stations, replacing one line-card controller and 33 High Level Data Link Controllers (HDLCs). It costs $18.10 (20,000). The PEB 2084H, a four-channel transceiver for the S/T interface, costs $17.50 (20,000). The PEB 2096H provides eight parallel, two-wire transceiver channels with a transmission range >1.3 km. It costs $28.10 (20,000). The PEB 2465H is a DSP-based, four-channel codec that lets you connect four analog telephones via IOM-2 interfaces to a digital PBX. The device includes all the circuits for encoding, decoding, and PCM filtering of four voice channels. It costs $12 (20,000). **Siemens Components Inc, Integrated Circuits Division**, Cupertino, CA. (408) 777-4500.
Circle No. 409

Multimedia interface chip connects a variety of devices. The ES968 contains dual game ports to connect two joysticks to a multimedia PC, enabling two people to play interactive games simultaneously. An MPU-401 serial port interfaces directly to a MIDI music synthesizer. The CD-ROM interface connects to IDE CD-ROMs and to several CD-ROMs with proprietary interfaces. The chip also supports Microsoft's add-in-card Plug and Play standard. The device comes in a 100-pin PQFP and costs $4.50. **ESS Technology Inc**, Fremont, CA. (510) 226-1088.
Circle No. 410

CAM provides user-configurable RAM with each entry. The MU9C1240 FastCAM provides associative caching at clock periods down to 50 nsec. The 128-entry content-addressable memory (CAM) has a 100-nsec compare cycle and a 50-nsec read/write cycle time. Nibble masking lets you configure the CAM width of each word from 24 to 48 bits and the corresponding RAM width from 7 to 31 bits in 4-bit increments. The devices come in a 44-pin PLCC or PQFP and cost $7.50 (1000). **Music Semiconductor**, Colorado Springs, CO. (719) 570-1550. **Circle No. 411**

32-bit graphics accelerator provides flicker-free output to NTSC/PAL TV monitors and VCRs. The TVG9470 TV accelerator interfaces to PCs using 32-bit Peripheral Component Interconnect, VL, and ISA buses. The graphics accelerator is based on the company's TGUI9440 graphics engine. According to the company, TV monitors have often been unusable for VGA graphics, PC games, and presentations due to the flicker effect. The new chip smoothes adjacent lines and eliminates single horizontal lines, which cause flicker on monitors using an interlaced display. The device costs $24 (1000). **Trident Microsystems Inc**, Mountain View, CA. (415) 691-9211.
Circle No. 412

3.3V FPGA family offers 1000 to 8000 gates. The CY7C338X family of field-programmable gate arrays (FPGAs) can implement loadable counters with operating frequencies >80 MHz and chip-to-chip operating frequencies up to 60 MHz. Prices for the 1000-gate CY7C3381A in a 44-pin PLCC start at $13.50 (100). Prices for the 4000-gate CY7C3385A in a 100-pin TQFP start at $41.15 (100). An 8000-gate device offering full PCI compliance will be available in the third quarter. **Cypress Semiconductor**, San Jose, CA. (408) 943-2600. **Circle No. 413**

622-Mbps SONET/ATM transceiver offers low power and low cost. The VSC8110 synchronous-optical-network (SONET)/asynchronous-transfer-mode (ATM) transceiver operates from 2 and 5V supplies with a 2W worst-case power dissipation. The SONET/synchronous-digital-hierarchy-compatible transceiver integrates high-speed clock generation with 8-bit serial-to-parallel and parallel-to-serial data conversion. The high-speed clock is generated using an on-chip PLL and is selectable for 155- or 622-MHz operation. It uses a reference clock of 19.44, 38.88, 51.84, or 77.76 MHz. The device comes in a 100-pin PQFP with an integrated heat spreader and costs $52 (1000). **Vitesse Semiconductor Corp**, Camarillo, CA. (805) 388-3700.
Circle No. 414

Single chip encodes MPEG-2 digital video pictures. The MPEG-2 encoder performs I-frame video compression. The encoder operates in 4:2:2 chroma format with CCIR 601 (720×480-pixel) resolution as well as in the 4:2:0 mode. The chip can sustain MPEG-2 I-frame-only compression data rates of greater than 40 Mbps. The 3.3V device comes in a 304-pin CQFP and costs $700 (50). An MPEG-2 decoder chip is also available. The chip can sustain MPEG-2 decompression data rates of >40 Mbps for I-frames and up to 15 Mbps for IPB frames. It comes in a 208-pin CQFP and costs $35 (OEM). **IBM Microelectronics**, Hopewell Junction, NY. (800) 769-3772.
Circle No. 415

Fast Ethernet transceiver offers 100-Mbps transmission over twisted-pair cable. The CY7C971 transceiver allows 100-Mbps transmission over category 3, 4, and 5 unshielded twisted-pair cable. It supports the 100BaseT4 Fast Ethernet standard, 10BaseT, and 10BaseT full-duplex. The

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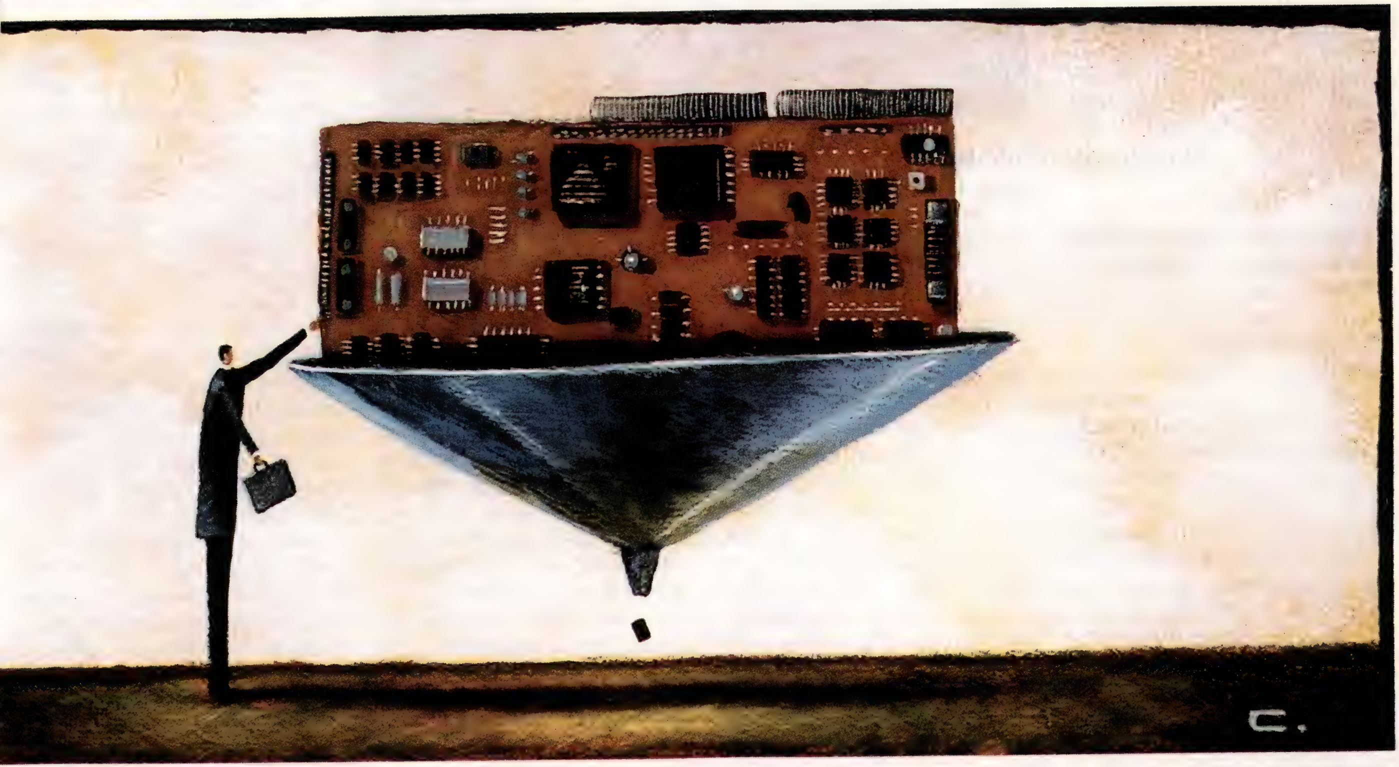

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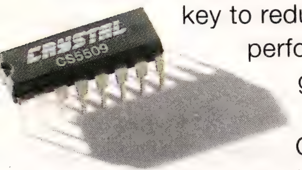

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CS5505	16	4	20/100
CS5506	20	4	20/60
CS5507	16	1	20/100
CS5508	20	1	20/60
CS5509	16	1	20/200

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device includes adaptive equalization, clock recovery, encoder/decoder functions, and transmit and receive filters. It comes in an 80-pin PQFP and costs $25 (1000). **Cypress Semiconductor**, San Jose, CA. (408) 943-2600.

Circle No. 416

μPs offer high-performance serial communications. The Z185/Z195 provide intelligent serial communications for network protocol conversion, high-speed faxes, modems, printer, bridges, and routers. The devices have two 512-kbps UARTs and two DMAs you can link to move data with less CPU intervention. The Z185 is a ROMless part and costs $12 (10,000). The Z195 is code-compatible with the Z80 and Z180. It costs $11 (10,000). Both come in 100-pin QFPs. The Z8018500ZCO evaluation board ($500) shortens code-development time. **Zilog**, Campbell, CA. (408) 370-8000. **Circle No. 417**

High-resolution CMOS, triple 256×8-bit RAMDACs offer 3-D modes. The Bt498 operates at up to 220 MHz, allowing it to accommodate 1600×1280-pixel displays at 76-Hz refresh rates. It has a 128-bit-wide pixel port. The Bt497 operates at up to 135 MHz, supporting 1280×1024-pixel displays at 75-Hz refresh rates. It has a 64-bit-wide pixel port. Both devices offer a double-buffering capability for 3-D applications, allowing you to display one complex image while updating the other. Samples of the Bt497 cost $58.67, and samples of the Bt498 cost $74.67. Volume production is scheduled for the second half of 1995. **Brooktree Corp**, San Diego, CA. (619) 452-7580.

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10-bit DAC provides 125-MHz conversion rate and 775-mW max power consumption. The HI5721 is pin-compatible with the AD5721 and provides a higher conversion speed and lower power consumption. The high conversion speed moves unwanted harmonics farther from the fundamental frequency in direct-digital-synthesis applications, simplifying lowpass-filter requirements. The device comes in a 28-lead PDIP or SOIC and costs $38 (100). **Harris Semiconductor**, Melbourne, FL. (800) 442-7747, ext 7334.

Circle No. 419

Video sync separator has improved performance and lower supply currents than the LM1881. The EL1881 is pin-compatible with the LM1881 yet requires only 1.5 mA from a 5V supply. The chip provides a precise 50% slicing for synchronous edge detection when the video input is 0.5 to 2V p-p. Available in an eight-pin DIP, the device costs $1.70 (1000). **Elantec Inc**, Milpitas, CA. (408) 945-1323. **Circle No. 420**

Programmable interconnect devices provide static or dynamic reconfiguration. The IQ96 and IQ64B provide 96 and 64 I/O ports, respectively. Both devices support 133-MHz clock rates and have a 6-nsec flow-through delay. The non-blocking, globally connected IQ architecture is a switch matrix that lets you connect any signal to one or more other signals. Each I/O port is identical and can be an input, an output, or a bidirectional port. The IQ96 costs $25 (10,000), and the IQ64 costs $17 (10,000). **I-Cube Inc**, Santa Clara, CA. (408) 986-1077.

Circle No. 421

Logic devices, buffers, and translators offer 250-psec propagation delay. The QuickSwitch devices offer pin-compatible replacements for logic buffers, multiplexers, demultiplexers, bus switches, bus exchangers, cross-bar switches, and other devices. According to the company, the high-speed devices may enable you to use slower SRAM without slowing system performance. A typical device in a QSOP costs $1.60 (1000). **Quality Semiconductor Inc**, Santa Clara, CA. (408) 450-8080.

Circle No. 422

Power module integrates power stage for 2- and 3-hp motor drives. The MHPM7A12A120 integrates a three-phase input rectifier bridge, a three-phase output inverter, a brake transistor/diode, a current-sense resistor, and a temperature sensor. The device is rated for 1200V and a continuous current of 12A. Typical V_{CE} is 2.4V. The module costs $65 (500). The MHPM7A16A120 is rated for 1200V and 16A continuous current. It costs $85 (500). The MHPM7A30A60 is rated for 600V and 30A continuous current. It costs $67 (500). **Motorola Semiconductor Products Sector**, Phoenix, AZ. (602) 244-4538. **Circle No. 423**

8-Mbit, 100-MHz, synchronous DRAM targets graphics applications. The HM5283206 is a 3.3V device organized as 256k×32 bits. The synchronous graphics RAM (SGRAM) maintains compatibility with the company's 2- and 4-Mbit synchronous DRAMs. The device offers block write and write mask, or "write-per-bit" functions. Although the device has a single port, its high speed and 32-bit width allow data transfers at up to 400 Mbytes/sec. Two devices configured for 64-bit bus applications offer 800-Mbyte/sec data transfers, exceeding typical VRAM configurations. The device comes in a 100-pin PQFP, and prices start at $39 (1000). The company plans volume production for the fourth quarter of 1995. **Hitachi America Ltd, Semiconductor & IC Division**, Brisbane, CA. (800) 285-1601, ext 11. **Circle No. 424**

18-bit×64-word FIFO buffers offer high-speed operation. The SY69167 performs one read or one write at up to 200 MHz. The SY69168 performs one read or one write at up to 100 MHz. Both 10KH-ECL-compatible devices come in 64-pin QFPs and cost $125 (1000). **Synergy Semiconductor**, Santa Clara, CA. (408) 730-1313.

Circle No. 425

256k×8-bit DRAM has 20-nsec EDO page-mode cycle time. The 2-Mbit V53C8258H DRAM has a 20-nsec extended-data-out (EDO) page-mode cycle time for Windows graphics-accelerator frame buffers. According to the company, the $9.50 (1000) device enables you to create high-performance frame buffers less expensively than with VRAMs. The device comes in

(continued on pg 145)

Switches, References and Multiplexers

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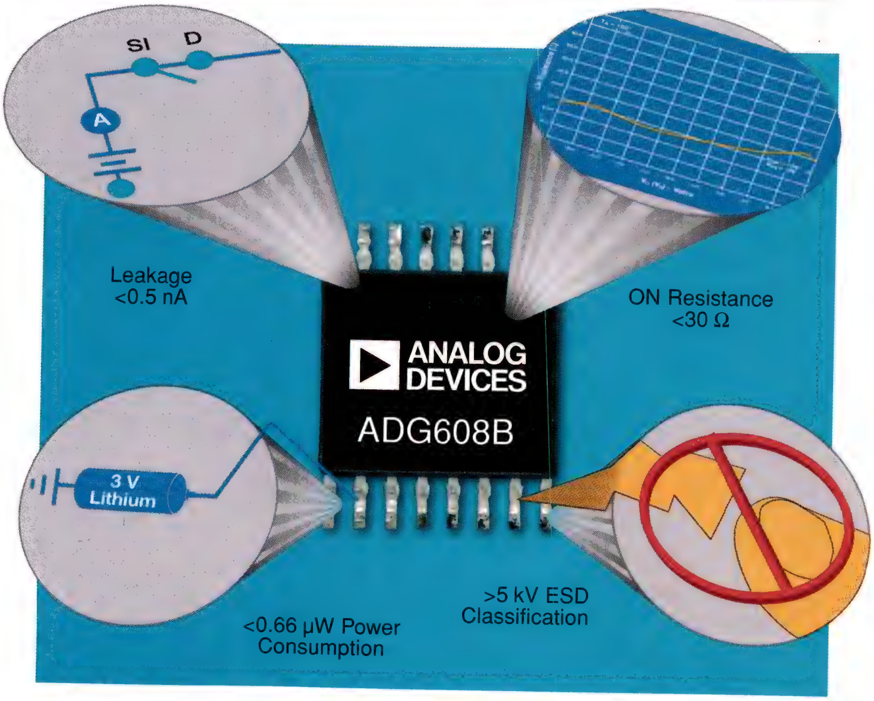

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The ADG608 and ADG609 are 8-channel and differential 4-channel multiplexers that are specified for +3 V, +5 V and ±5 V power supplies. Offering a combination of very low ON resistance (less than 30 Ω) and low leakage current (less than 0.5 nA), the ADG608 and ADG609 are ideal for use in precision applications which previously required several additional components.

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- Power consumption ranges from as low as 0.1 µW with a single +3 V power supply to 1.5 µW with dual 5 V supplies.
- State-of-the-art 16-lead TSSOP packaging that meets the limitations of the PCMCIA release 3 standard specifications. It occupies only 51 k sq. mils of board space — which is roughly half that of a 16-lead narrow-body SOIC package — and has a package height of only 39 mils.

With an ESD classification of greater than 5 kV and latchup-free operation to at least 100 mA, reliability is built in. ESD classification is carried out per the military standard 3015.7.

These multiplexers are available in 16-pin DIP and TSSOP packages specified over the -40 to +85° C temperature range as well as a TSSOP package specified over the -55 to +125° C range.

(continued on page 2)

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†All prices shown in USD, 1000s, recommended resale, FOB USA

+3 V/+5 V Specified Switches and Multiplexers

World's First +3 V/+5 V Multiplexer

(continued from page 1)

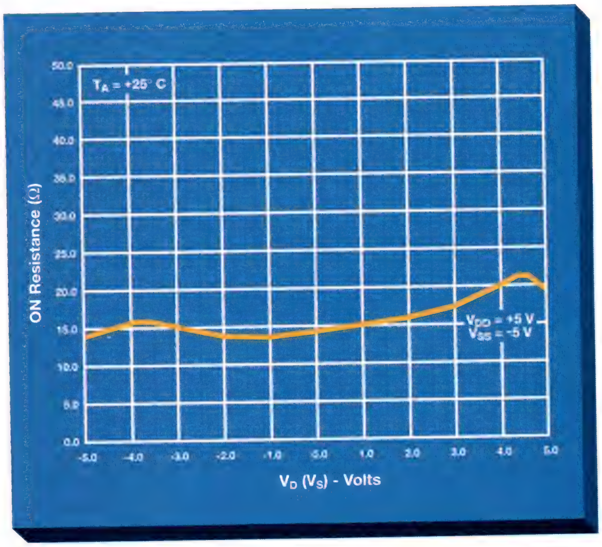
ADG608/ADG609 Specifications

Power Supply	±5 V	+5 V	+3 V
R_{on}	30 Ω max	50 Ω max	90 Ω max
ON Leakage	±0.5 nA max	±0.5 nA max	±0.5 nA max
t_{on}	75 ns max	100 ns max	170 ns max
Charge Injection	6 pC typ	0.5 pC typ/ 3 pC max	0.5 pC typ/ 3 pC max
I_{dd}	0.2 μA max	0.2 μA max	0.2 μA max

KEY FEATURES

- +3 V, +5 V, ±5 V specifications
- 1.5 μW max power dissipation
- 30 Ω max on resistance
- ESD classification greater than 5 kV

ADG608	Price $3.25	Faxcode 1912	Circle 01
ADG609	Price $3.25	Faxcode 1912	Circle 02



World's Only Latchup-Free Switch Specified at Single Supply +3 V/+5 V

The ADG511 family of quad SPST switches is the world's first and only series of switches specified for +3 V, +5 V and ±5 V supplies that guarantees latchup-free operation. The family includes the ADG511 which has four NC; the ADG512 which has four NO; and the ADG513 which has two NO and two NC switches. Low ON resistance (<50 Ω), low leakage current (less than 100 pA) and fast switching times (t_{on} < 35 ns; t_{off} < 150 ns) make these switches ideal for high-resolution data acquisition systems and signal conditioning applications. Also, the requirement for low power dissipation in battery-powered applications can be easily solved by the ADG511 family of switches with their typical power dissipation of 0.5 nW.

These switches are available in 16-pin DIP and SOIC packages specified over the -40 to +85° C temperature range and a cerdip package specified over the -55 to +125° C range.

KEY FEATURES

- Specified with +3 V, +5 V, ±5 V power supplies
- Guaranteed NEVER to latchup
- Industry standard pin-out

ADG511	Price $2.05	Faxcode 1520	Circle 03
ADG512	Price $2.05	Faxcode 1521	Circle 04
ADG513	Price $2.05	Faxcode 1522	Circle 05

Selection Guide for CMOS Switches and Multiplexers

This new 12-page brochure contains selection trees and product charts for choosing the correct analog switch or multiplexer for your design. Parts which offer:

- Trench Isolation
- Low Power Consumption
- Fault Protection
- High-Speed Performance

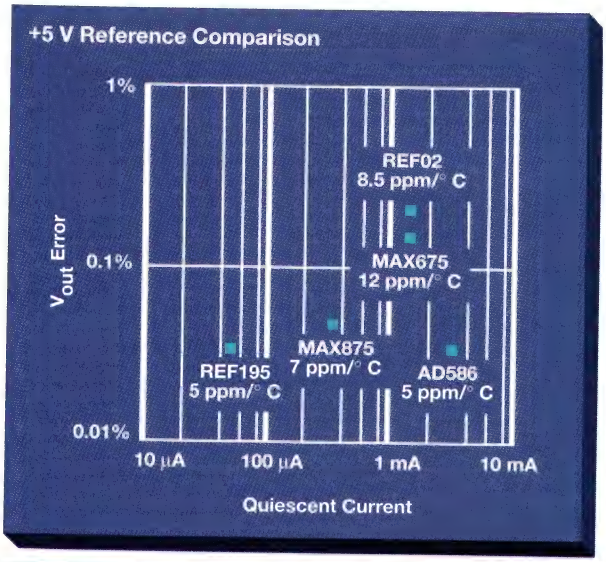
To get your FREE copy, please complete and return the enclosed reply card.

CMOS Switch and Multiplexer Selection Guide Circle 06

New Voltage References Guarantee Precision and Micropower Operation

The REF19X family of precision voltage references features low dropout voltage, micropower consumption and sleep mode. Applications for the seven family members include A/D reference, loop-powered instruments and micropower voltage regulators. The REF191/2/4/5/8 outputs +2.048 V, +2.5 V, +4.5 V, +5.0 V and +4.096 V respectively, with ±2 mV initial accuracy and 5 ppm/° C temperature coefficient (E grade). The REF193 and REF196 outputs +3 V and +3.3 V respectively, with ±10 mV initial accuracy and 25 ppm/° C tempco. All devices feature a 30 mA max load current and 45 µA max quiescent current with less than 15 µA in sleep mode. Devices are packaged in 8-pin SO and DIP and are specified from -40 to +85° C. Pricing starts at $1.91 in SO-8 for all voltage options.

REF191	Priced From $1.91	Faxcode 1761	Circle 07
REF192	Priced From $1.91	Faxcode 1761	Circle 08
REF193	Priced From $1.91	Faxcode 1761	Circle 09
REF196	Priced From $1.91	Faxcode 1761	Circle 10
REF198	Priced From $1.91	Faxcode 1761	Circle 11
REF194	Priced From $1.91	Faxcode 1761	Circle 12
REF195	Priced From $1.91	Faxcode 1761	Circle 13

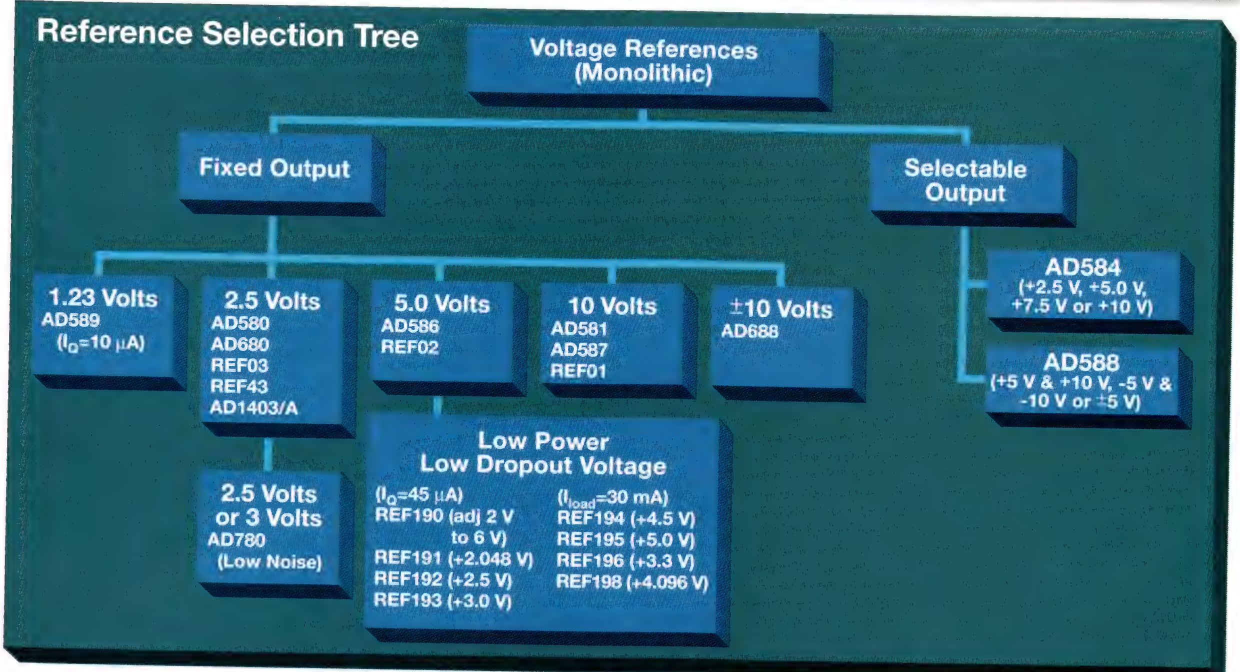


KEY FEATURES
- Tight initial accuracy ±2 mV max.
- 5 ppm/° C max temperature coefficient
- 45 µA quiescent current, 15 µA in sleep mode

REF19X SELECTION GUIDE

	Output Voltage (V)	Accuracy (mV Max)	Tempco (ppm/° C Max)	Line Regulation (ppm/V Max)	Dropout Voltage (mV)
REF191	2.048	±2, ±5, ±10	5, 10, 25	4, 8, 8	650
REF192	2.500	±2, ±5, ±10	5, 10, 25	4, 8, 8	500
REF193	3.000	±10	25	8	300
REF196	3.300	±10	25	8	200
REF198	4.096	±2, ±5, ±10	5, 10, 25	4, 8, 8	200
REF194	4.500	±2, ±5, ±10	5, 10, 25	4, 8, 8	250
REF195	5.000	±2, ±5, ±10	5, 10, 25	4, 8, 8	100

Reference Selection Tree



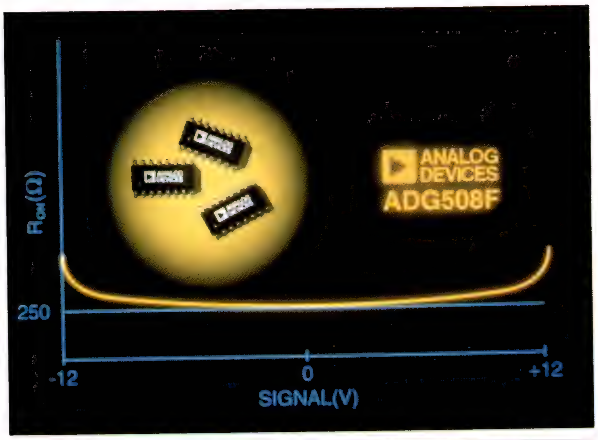
World's Highest Performance Fault-Protected Multiplexers

New

Trade In All Your Multiplexer Trade Offs

The ADG508F family combines fault protection with the performance of existing non-fault protected multiplexers. The ADG508F and ADG528F are 8-channel multiplexers and the ADG509F is a differential 4-channel multiplexer. In addition to 8 channels, the ADG528F has on-chip address and control latches. These multiplexers are protected against overvoltage up to ±35 V as well as power supply loss conditions. The ON channel switches off while an overvoltage exists, thereby protecting downstream devices. If the power supply is disconnected, all the channels switch off. The ADG508F ON resistance is 300 Ω typical and has a maximum ON leakage — over the full industrial temperature range — of ±60 nA. This represents about a five times performance improvement over existing fault-protected multiplexers. Power consumption is also significantly reduced with an I_{dd} of 0.5 mA and I_{ss} of 0.1 mA. The entire ADG508F family features typical t_{on} and t_{off} times of 200 ns and typical charge injection of 4 pC.

These multiplexers are available in 16-pin DIP as well as narrow- and wide-body SOIC packages specified over the -40 to +85° C temperature range. A cerdip package specified over -55 to +125° C is also available.



KEY FEATURES

- Overvoltage and fault protection
- No performance trade offs
- Narrow-body SOIC package available

ADG508F	Price $3.35	Faxcode 1845	Circle 14
ADG509F	Price $3.35	Faxcode 1845	Circle 15
ADG528F	Price $3.85	Faxcode 1845	Circle 16

New

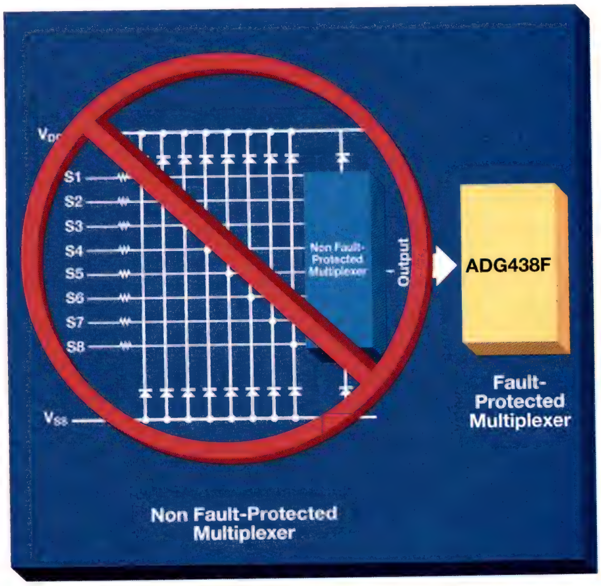
High-Performance Fault-Protected Multiplexers

The ADG438F and ADG439F are high-performance multiplexers protected against overvoltages of -35 V to +50 V. Not only are the multiplexers themselves protected against overvoltage and fault conditions, but so are any downstream devices because the output of the multiplexer is clamped below the power rail. If this power rail is zero due to momentary power loss, then the output will be clamped at zero. Only the channel on which the overvoltage occurs is clamped, all other channels remain unaffected.

With an ON resistance of 400 Ω, ON resistance match of 3 Ω max and Δ ON resistance of 5 Ω max over the extended industrial temperature range of -40 to +105° C, the performance of the ADG438F and ADG439F exceeds all the fault-protected and the majority of non-fault-protected multiplexers currently on the market.

These multiplexers are available in 16-pin DIP and both wide- and narrow-body SOIC packages.

Parameter	ADG438F	ADG439F
R_{on}	400 Ω max	400 Ω max
R_{on} Match	5 Ω max	5 Ω max
Delta R_{on}	3 Ω max	3 Ω max
ON Leakage	±30 nA max	±15 nA max
t_{on}	300 ns max	300 ns max
I_{dd}	0.25 mA max	0.25 mA max


V_{DD}
S1
S2
S3
S4
S5
S6
S7
S8
V_{SS}
Non Fault-Protected Multiplexer
Output
ADG438F
Fault-Protected Multiplexer
Non Fault-Protected Multiplexer

KEY FEATURES

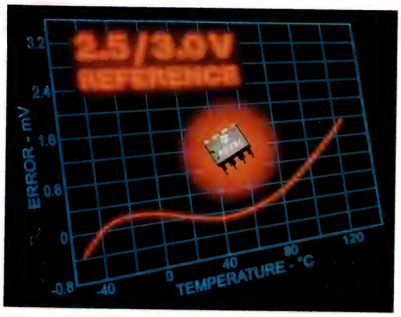
- Overvoltage and fault protection (-35 V to +50 V)
- Extended industrial temperature range (-40 to +105° C)
- Narrow-body SOIC package available

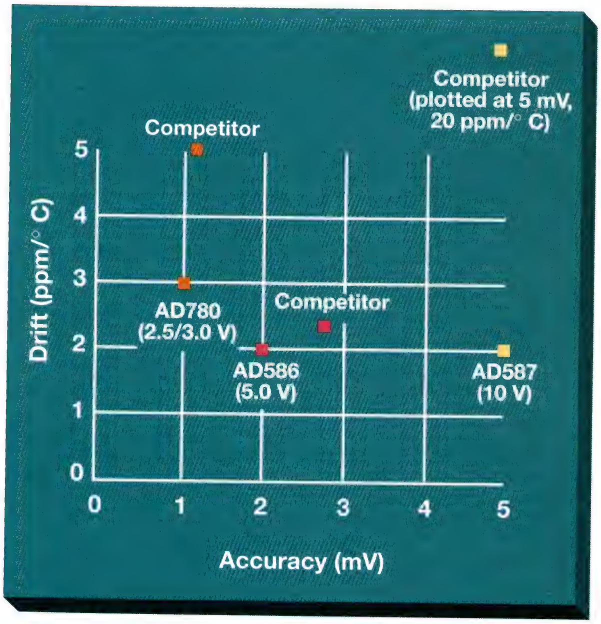
ADG438F	Price $3.70	Faxcode 1855	Circle 17
ADG439F	Price $3.70	Faxcode 1855	Circle 18

Compact References with Precision Performance

High Accuracy, Low Noise Precision References

The AD780, AD586, and AD587 precision voltage references comprise the highest accuracy and lowest noise +2.5 V, +5 V, and +10 V parts in existence. With drift performances from 2 ppm/°C, initial accuracies of ±1 mV and wideband noise as low as 100 nV/√Hz, these products should be the first choice for all high-performance applications. They are available in a wide variety of performance grades, package styles and temperature ranges, making it easy to choose exactly the right part to meet the performance and cost requirements of any application.





KEY FEATURES
- High accuracy and low noise
- Drift performance from as low as 2 ppm/° C
- Variety of grades and packages available

AD780	Priced from $3.31	Faxcode 1355	Circle 19
AD586	Priced from $2.50	Faxcode 1182	Circle 20
AD587	Priced from $2.20	Faxcode 1183	Circle 21

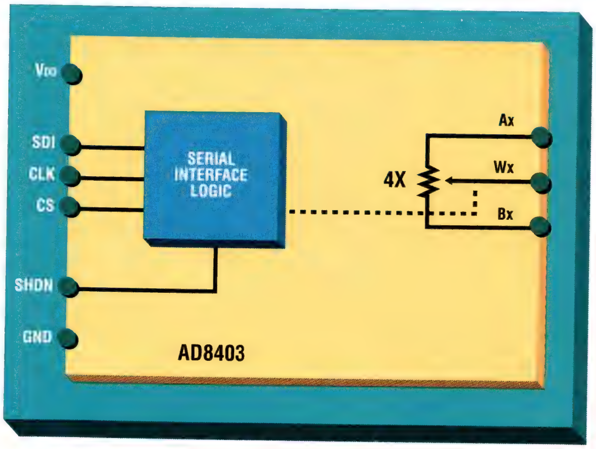
Part #	Drift (ppm/° C)	Initial Accuracy (mV)	Wideband Noise (nV/√Hz)	Packages
AD780	3-7	1-5	100	SOIC, PDIP, CERDIP
AD586	2-25	2-20	100	SOIC, PDIP, CERDIP
AD587	2-20	5-10	100	SOIC, PDIP, CERDIP

Digital Potentiometers

New

Dual and Quad 8-Bit Digital Potentiometers

Want to replace your mechanical potentiometers with more precise and accurate devices? Then try our solid-state dual- (AD8402) and quad- (AD8403) channel 8-bit RDACs (Resistor Digital-to-Analog Converters). They are a set of 256 position, digitally-controlled variable resistors which operate from +2.7 V to +5.5 V in single-supply systems with rail-to-rail signal range. These RDACs can be used as programmable filters, delays or time constants, volume controls, DC gain/offset adjustments and line impedance matching components.



KEY FEATURES
- Digitally controlled resistance
- Mid-scale reset
- Power shutdown <5 µA

AD8402	Price $1.66	Faxcode 1867	Circle 22
AD8403	Price $2.51	Faxcode 1867	Circle 23

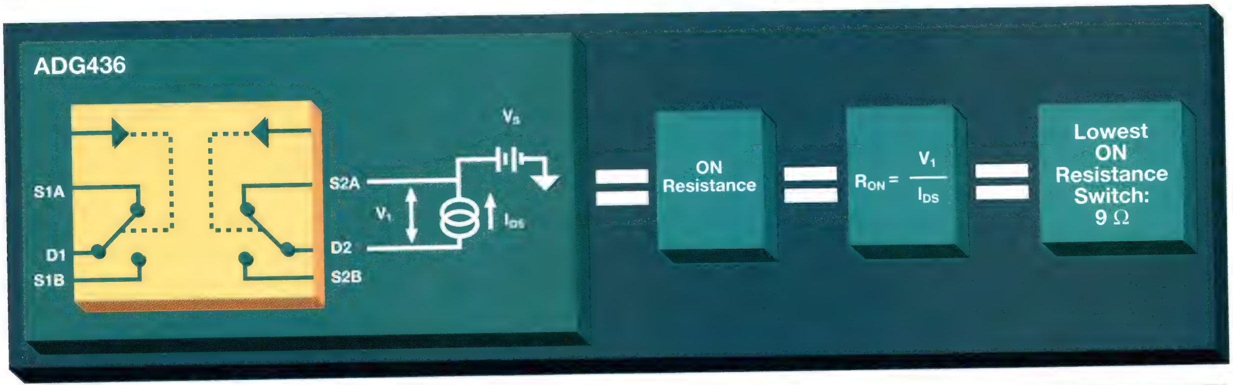
World's Lowest R_{ON} CMOS Switches

Dual SPDT Switch Has ON Resistance of 9 Ω

The ADG436 is a high-performance, dual SPDT switch. It offers a level of performance that has previously been unavailable in any switch format. With a typical ON resistance of 9 Ω and leakage current of 0.1 nA, the ADG436 makes it possible to use a switch in many high-performance applications that previously required several extra components. The SPDT switch function can also be thought of as a two-channel multiplexer, allowing the ADG436 to be used as a dual two-channel multiplexer. While specified for a single +12 V supply as well as ±15 V with 10% tolerance, the ADG436 can operate with supplies as low as +3 V or as high as ±20 V. The typical power consumption is 3 nW. With such low power consumption and the ability to operate from a single +3 V or +5 V supply, this switch is an ideal candidate for portable and battery-operated systems. Parts are available in 16-pin DIP and SOIC packages specified over the -40 to +85° C temperature range.

KEY FEATURES
- 9 Ω typical ON resistance
- Typical power consumption of 3 nW
- Operates with power supplies from +3 V to ±20 V

ADG436	Price $2.50	Faxcode 1918	Circle 24


ADG436
S1A
D1
S1B
S2A
D2
S2B
V_S
V_1
I_{DS}
ON Resistance
$R_{ON} = \frac{V_1}{I_{DS}}$
Lowest ON Resistance Switch: 9 Ω

Quad Rail-To-Rail SPST Switch has Less Than 24 Ω ON Resistance

This high-performance quad SPST switch family includes the ADG431 which has four NC; the ADG432 which has four NO; and the ADG433 which has two NO and two NC switches. Applications that use switches in the signal path must keep the error introduced by leakage currents and extra resistance to a minimum. With ON resistance of less than 24 Ω and leakage of less than 0.35 nA, these are the only quad CMOS switches available that truly offer the performance you need. And, at only 3 μW power consumption (typical) from power supplies of ±15 V, you don't have to compromise. The ADG431 family can also boast a t_{on} time of 165 ns max. over the industrial temperature range of -40 to +85° C, and all are available in 16-pin DIP and SOIC packages. A cerdip package specified over the -55 to +125° C range is also available.

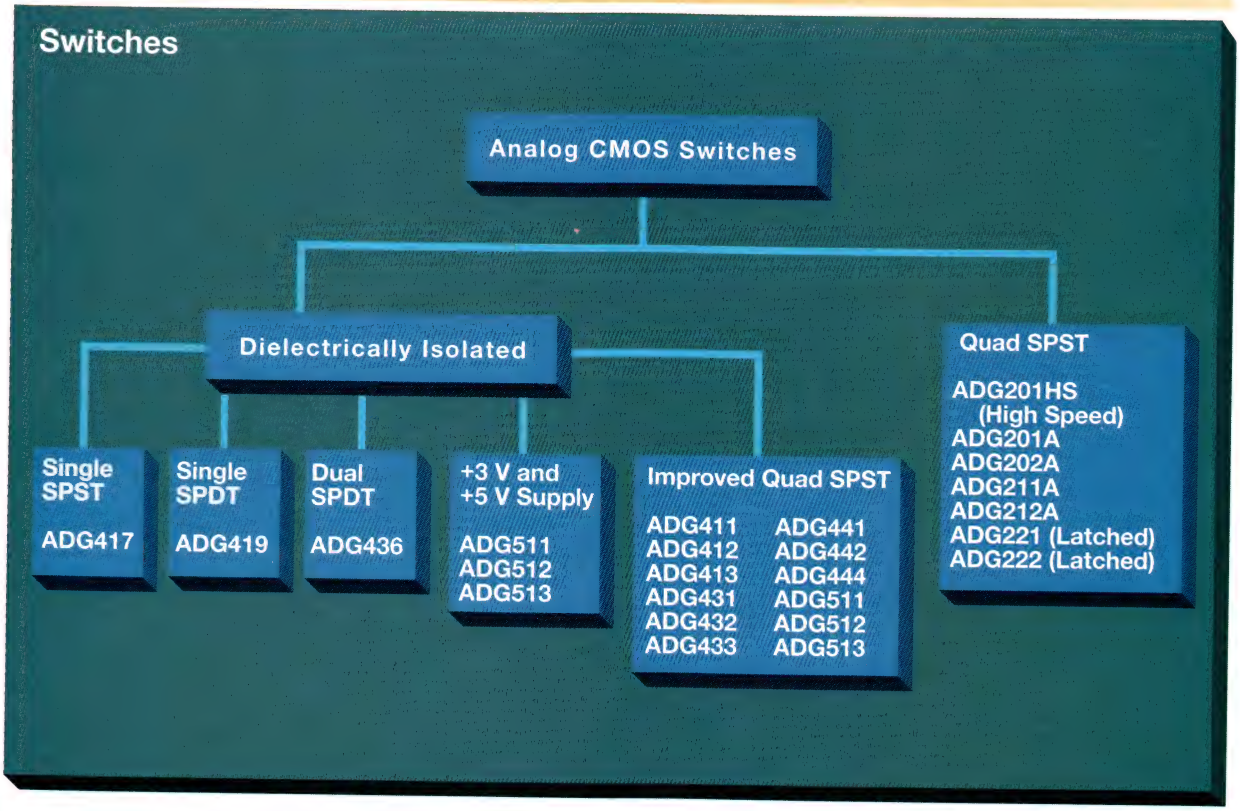
KEY FEATURES
- Highest-performance quad SPST available
- Guaranteed to NEVER latchup
- Industry standard pin out

ADG431	Price $1.95	Faxcode 1510	Circle 25
ADG432	Price $1.95	Faxcode 1511	Circle 26
ADG433	Price $1.95	Faxcode 1512	Circle 27

LARGEST AVAILABILITY OF SMALLEST PACKAGES

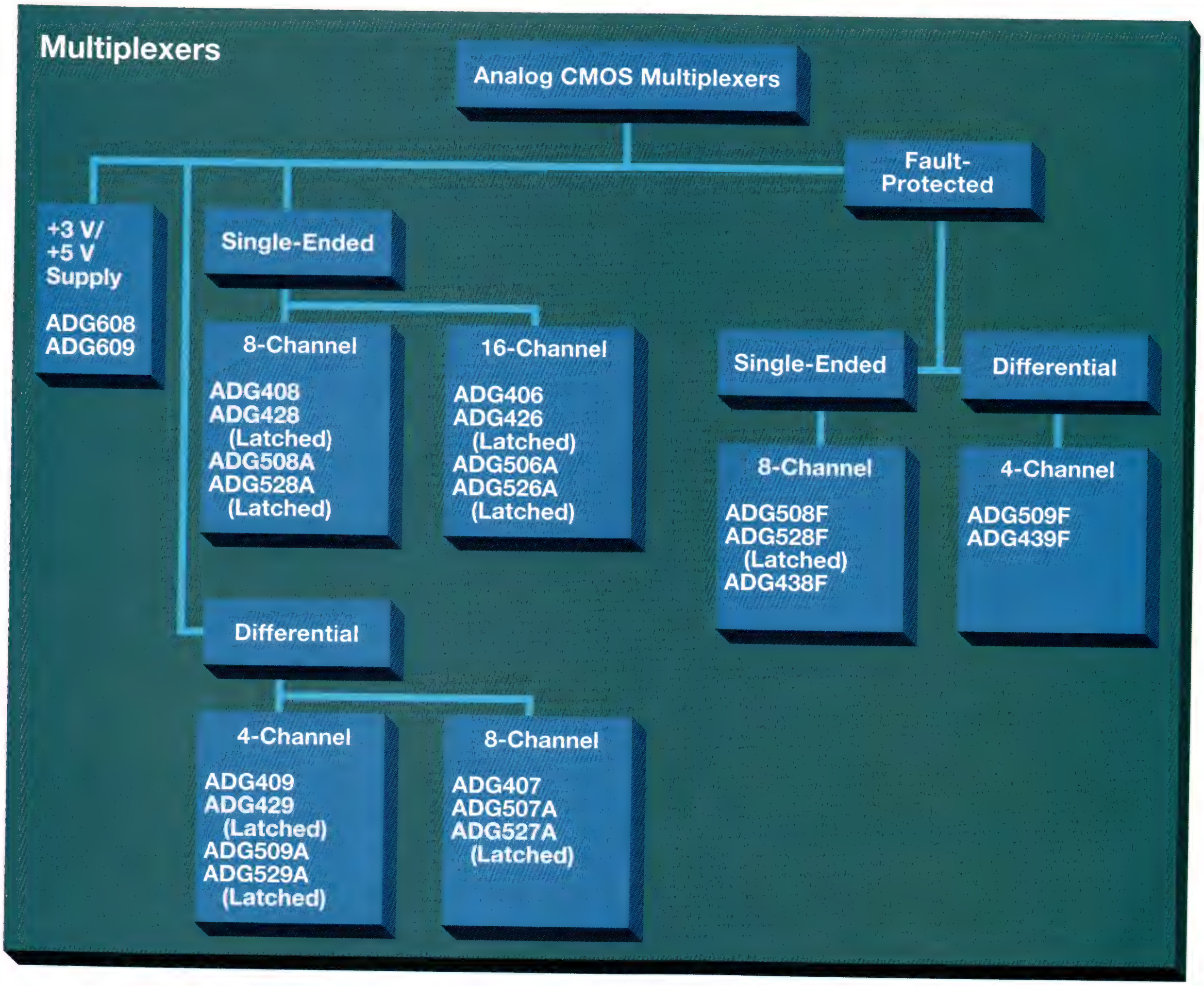
Package Dimensions (mils)	16-lead TSSOP ADG608/ADG609	8-pin SOIC ADG417/ADG419	28-lead SSOP ADG426	20-lead SSOP ADG511
Body Length	201	196	407	289
Body Width	176	157	212	212
Tip to Tip	256	244	311	311
Pitch	25	50	25	25
Package Height	39	68.8	78	78
Board Area	51 k	47 k	126 k	90 k

Switch and Multiplexer Selection Trees



Switches

- Analog CMOS Switches
  - Dielectrically Isolated
    - Single SPST
      - ADG417
    - Single SPDT
      - ADG419
    - Dual SPDT
      - ADG436
    - +3 V and +5 V Supply
      - ADG511
      - ADG512
      - ADG513
    - Improved Quad SPST
      - ADG411
      - ADG412
      - ADG413
      - ADG431
      - ADG432
      - ADG433
      - ADG441
      - ADG442
      - ADG444
      - ADG511
      - ADG512
      - ADG513
  - Quad SPST
    - ADG201HS (High Speed)
    - ADG201A
    - ADG202A
    - ADG211A
    - ADG212A
    - ADG221 (Latched)
    - ADG222 (Latched)



Multiplexers

- Analog CMOS Multiplexers
  - +3 V/ +5 V Supply
    - ADG608
    - ADG609
  - Single-Ended
    - 8-Channel
      - ADG408
      - ADG428 (Latched)
      - ADG508A
      - ADG528A (Latched)
    - 16-Channel
      - ADG406
      - ADG426 (Latched)
      - ADG506A
      - ADG526A (Latched)
  - Differential
    - 4-Channel
      - ADG409
      - ADG429 (Latched)
      - ADG509A
      - ADG529A (Latched)
    - 8-Channel
      - ADG407
      - ADG507A
      - ADG527A (Latched)
  - Fault-Protected
    - Single-Ended
      - 8-Channel
        - ADG508F
        - ADG528F (Latched)
        - ADG438F
    - Differential
      - 4-Channel
        - ADG509F
        - ADG439F

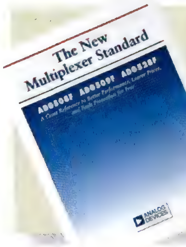
Switch and Multiplexer Summary Guides

SWITCHES

PARAMETER		ADG201A	ADG201AHS	ADG211A	ADG411	ADG431	ADG441	ADG444	ADG511	ADG419
ON Resistance (Ω)	25° C	90	50	115	35	24	75	75		35
	Tmin to Tmax	145	75	175	45	26	85	85	50	45
Channel ON Leakage (nA)	25° C	±2	±1	±5	±0.4	±0.35	±0.5	±0.5	±0.2	±0.75
	Tmin to Tmax	±200	±20	±200	±40	±2	±3	±3	±5	±5
Turn-On Time (ns)	25° C	300	50	600			110	110		
	Tmin to Tmax		50		175	165	170	170	375	
Turn-Off Time (ns)	25° C	250	50	450			60	60		
	Tmin to Tmax		50		145	130	80	80	150	
Charge Injection (pC)	25 °C typ	20	10	20	5	5	1	1	11	
	25° C max						6	6		
Positive Supply Current	25° C		10 mA		1 µA	0.1 µA		1 µA		1 µA
	Tmin to Tmax	2 mA	10 mA	1 mA	5 µA	0.2 µA	80 µA	2.5 µA	1 µA	2.5 µA
Negative Supply Current	25°C		6 mA		1 µA	0.1 µA	1 µA	1 µA		1 µA
	Tmin to Tmax	0.2 mA	6 mA	0.2 mA	5 µA	0.2 µA	2.5 µA	2.5 µA	1 µA	2.5 µA
Logic Supply Current	25°C				1 µA	0.1 µA		1 µA		1 µA
	Tmin to Tmax			0.9 mA	5 µA	0.2 µA		2.5 µA		2.5 µA

MULTIPLEXERS

PARAMETER		ADG406	ADG408	ADG426	ADG428	ADG506A	ADG508A	ADG528A	ADG526A ADG508F	ADG438F	ADG608
ON Resistance (Ω)	25° C	80	100	80	100	450	450	450			30
	Tmin to Tmax	125	125	125	125	600	600	600	400	400	35
Channel ON Leakage (nA)	25° C	±1	±1	±1	±1	±1	±1	±1	±1	0.5	±0.5
	Tmin to Tmax	±20	±100	±20	±100	±200	±100	±200	±60	±5	±3
Turn-On Time (ns)	25° C	160	150	160	150	300	300	300	250	250	75
	Tmin to Tmax	225	225	225	225	400	400	400	400	300	90
Turn-Off Time (ns)	25° C	150		150	150	300	300	300	250	150	45
	Tmin to Tmax	180	150	180	300	400	400	400	400	180	60
Charge Injection (pC)	25° C typ	8	20	8	4	4	4	4	4	4	0.5 3
Positive Supply Current	25° C	1 µA	1 µA	1 µA						0.15 mA	0.2 µA
	Tmin to Tmax	5 µA	5 µA	5 µA	0.1 mA	1.5 mA	1.5 mA	1.5 mA	0.2 mA	0.25 mA	2 µA
Negative Supply Current	25° C	1 µA	1 µA	1 µA						0.02 mA	0.1 µA
	Tmin to Tmax	5 µA	5 µA	5 µA	5 µA	0.2 mA	0.2 mA	0.2 mA	0.1 mA	0.04 mA	1 µA



New Cross-Reference Guide and Fault-Protection Brochure

Want to learn more about the benefits of FREE fault protection? Need a handy chart for cross references? Our new 6-page brochure contains all the information required to specify a multiplexer with full fault protection. To receive your copy, please complete and return the enclosed reply card.

The New Multiplexer Standard Circle 28

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24-pin PDIP and 26/24-lead SOJ packages. **Mosel Vitelic**, San Jose, CA. (408) 433-6000. **Circle No. 426**

512k×8-bit SRAM suits military and high-reliability applications. The 4-Mbit EDI88512C SRAM comes in 55-, 70-, 85-, and 100-nsec speeds. All inputs and outputs are TTL-compatible, and the chip operates from a 5V supply. A low-power option provides battery backup for 2V data retention. The MIL-STD-883-compliant device comes in a ceramic, 600-mil DIP. It costs $418 (100) for the 55-nsec speed to $379 (100) for the 100-nsec speed. **Electronic Designs Inc**, Westborough, MA. (508) 366-5151. **Circle No. 427**

Synchronous DRAM and modules using the SDRAM suit main-memory applications. The 16-Mbit HM5216805 is a 3.3V device organized as two banks of 1M×8 bits. It is available in versions with speeds up to 100 MHz. The device comes in a 44-pin plastic TSOP-II and costs $60 (1000). The HB526A272F module uses nine of the memories organized as a 2M×72-bit dual in-line memory module to achieve data-transfer speeds up to 900 Mbytes/sec. The module costs $650 (1000). **Hitachi America Ltd, Semiconductor & IC Division**, Brisbane, CA. (800) 285-1601, ext 11. **Circle No. 428**

64-bit accelerator for Windows runs 25% faster than its predecessor. The M3145A AliCAT-64 graphics accelerator offers performance >30 million Winmarks. The chip interfaces directly to VL and PCI bus designs without extra logic and includes drivers for Windows 3.1, Windows NT, and OS/2 versions 2.x and 3.0. The device comes in a 208-pin PQFP and costs $9.50. **Acer Laboratories Inc, Pacific Technology Group**, Santa Clara, CA. (408) 764-0644. **Circle No. 429**

Cache modules for Pentium-processor-based systems. The IDT7MPV6214/15 cache modules for bus speeds to 66 MHz work with the OPTi Viper core-logic chip-set family. The modules let you add a 256- or 512-kbyte, asynchronous secondary cache to a system design with minimal effort. The modules use the company's 32k×8-bit, 3.3V 71V256 SRAMs and have a 160-lead, low-profile card edge package. The modules start at $72 (1000). **Integrated Device Technology Inc**, Santa Clara, CA. (800) 345-7015. **Circle No. 430**

16-Mbit SRAM modules meet military specifications. The WS512K32 family of CMOS memory modules is available with access times from 20 to 120 nsec. They meet MIL-H-38534 and MIL-STD-883. The memory modules have TTL-compatible levels and operate from 5V. The memories have a maximum supply current of 4 mA in standby mode. The 32-bit-wide memories are available in a surface-mount, 68-pin CQFP or a 66-pin pin-grid array. Military models start at $1700 (100). **White Microelectronics**, Phoenix, AZ. (602) 437-1520. **Circle No. 431**

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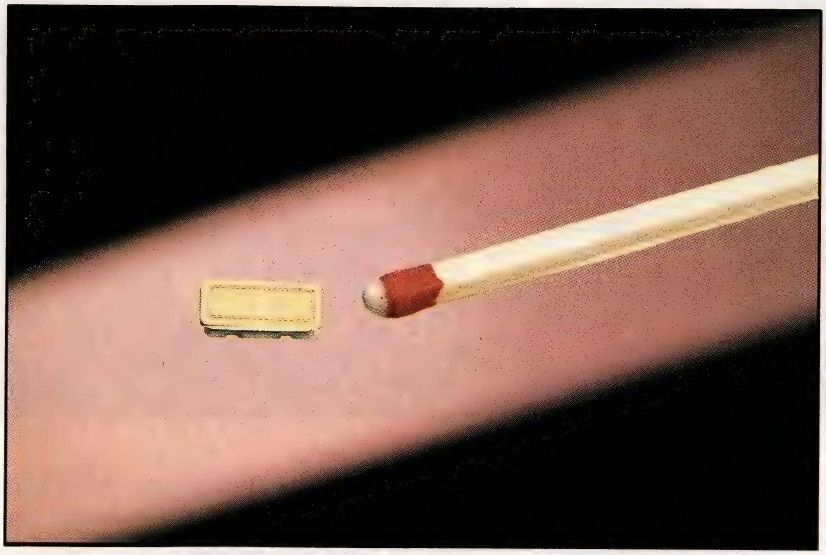

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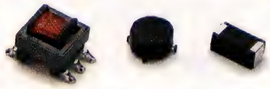
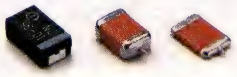
CIRCLE NO. 32

(MAX724 schematic courtesy of Maxim Integrated Products)

Our passives can help you meet the challenges of converting low voltages and extending battery life. Take a look at any schematic for these applications. Discover how quickly we can surround your IC with all the right surface mounted capacitors, resistors, magnetic components. Discover the efficiency of an integrated source able to shorten your time to market. For technical information, call Vishay Electronic Components, U.S. at one of the numbers below. For literature only, fax 1-800-835-4272.



MAGNETICS
Inductors/Transformers for filtering and energy storage. Wide range of standard models plus fast turnaround on custom designs. Phone Dale Electronics, Inc., (605) 665-9301 (Yankton, SD).



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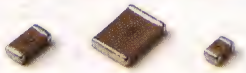

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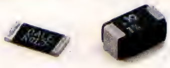

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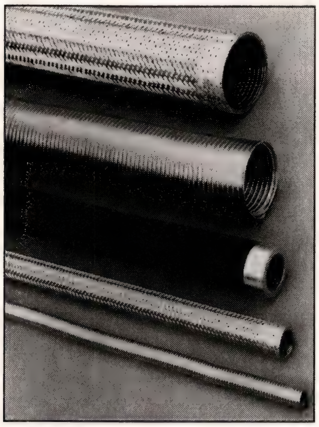
Flexible metal conduit provides shielding that meets military and IEEE nuclear specifications. The ServicAir shielding-product group features flexible metal conduits, coupling systems, shielded cable/harness assemblies, and custom shielding products. The watertight, pressure-tight conduits provide protection from transient interference, pulses and unwanted frequencies, and physical or environmental damage. The products provide up to 130 dB of EMI and up to 100 dB of plain-wave electromagnetic-pulse shielding. The SM83-03NC nickel-iron conduit costs $7.81/ft (300 ft). **G&H Technology Inc**, Camarillo, CA. (805) 484-0543. **Circle No. 352**



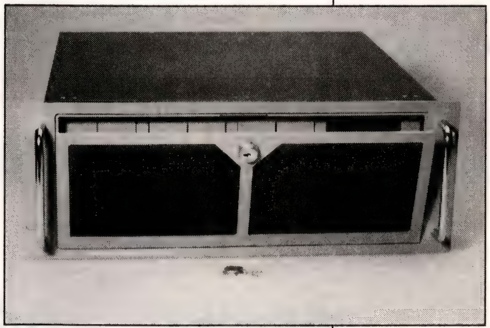
Low-cost 1300-nm laser diodes. The ML776H8F and ML77K8F laser diodes cost $60 (100), and the FU-427SLD laser diode module costs $175 (100). All three devices have a typical threshold current of 10 mA and typical operating current of 19 mA. The devices provide high-speed response for use in 155- to 622-Mbyte/sec transmission systems and can be qualified to the Bellcore reliability standards. Operating temperature range is –40 to +85°C. **Mitsubishi Electronics America Inc**, Sunnyvale, CA. (408) 730-5900. **Circle No. 353**

Large-digit counters are visible for up to 100 ft. The large-digit counters use 1.8-in. high LEDs for high visibility. Maximum count rate is 10 kHz. The units require 110 or 220V ac and provide a 12V-dc output for powering a sensor. The three-digit model costs $169, and the six-digit model costs $199. **Automated Control Systems**, Los Angeles, CA. (310) 659-2786. **Circle No. 354**

Oven-controlled crystal oscillator provides high stability. The 10-MHz 260-0536 oscillator uses an SC-cut resonator with thermal stability of $\pm1\times10^{-9}$ from –30 to +70°C. Optional thermal stabilities are available to $\pm1\times10^{-10}$. Aging is specified at 3×10^{-10} per day and 5×10^{-8} per year. Phase noise at 10-Hz offset is –125 dBc/Hz, with a noise floor of –60 dBc/Hz. The device measures 2×2×1.5 in. and costs $480. **Milliren Technologies Inc**, Newburyport, MA. (508) 465-6064. **Circle No. 355**

15-slot backplane increases PC-hardware interrupt capacity by four times. More interrupts on the IEF15-I overcome the limitation of a standard PC bus backplane. In a standard PC bus architecture, system-overhead functions consume most of the interrupts, leaving few for application use. The Interrupt Expansion Facility backplane provides more interrupts and maintains compatibility with standard ISA bus cards. The backplane, including system software, costs $995. **Little Wing Technologies Inc**, San Diego, CA. (619) 457-0581. **Circle No. 356**

Computer cable with 90° slim-line connector fits into your pocket. The Flexi-Lite cable line for portable computers or systems with limited space around cable connectors combines a 90° connector with super-flexible cable. Cables come in DB-9 serial, DB-25 serial, AT serial, and parallel-printer configurations. The fully shielded cables are made of molded 29 AWG cable. The cables cost $8 to $12, depending on length and configuration. **Unicom Electric Inc**, Santa Fe Springs, CA. (310) 946-9650. **Circle No. 357**



▲Rack-mount drive bays suit SCSI I/O connections. The 6531-RMDB provides four drive bays that accommodate eight half-height drives or four full-height drives. Each of the two 150W 120/220V-ac-selectable power supplies has a separate on/off switch, and the chassis has a 60-cfm filtered input fan and the power-supply fans. The drive bay costs $695. The 6531-RMDBD is functionally similar but adds a hinged front panel with a window and a key lock for security. It costs $895. Both models provide a rear-panel knockout for SCSI I/O connections for daisy-chaining additional drive bays. **Industrial Computer Source**, San Diego, CA. (800) 523-2320. **Circle No. 358**

Compact bias tee operates from 10 to 1000 MHz. The PBTC-1G bias tee has a typical insertion loss of 0.6 dB. It accepts a maximum input current of 500 mA and has a maximum RF power rating of 30 dBm. The case measures 0.8×0.8×0.4 in. The device costs $25.95. **Mini-Circuits**, Brooklyn, NY. (718) 934-4500. **Circle No. 359**

Surface-mount connector sets have 0.025-in. pitch. The high-density, four-row, FOLC series sockets and MOLC series terminal strips terminate on two rows. The sockets use three-finger beryllium copper contacts and mate with phosphor bronze terminals. The connectors form a matched-impedance connection for high-speed applications. Connector sets are available in pin counts from 20 to 50 per row. Optional locking clips and pick-and-place pads facilitate assembly. From $0.15 per mated line. **Samtec Inc**, New Albany, IN. (812) 944-6733. **Circle No. 360**

Barrier-terminal strip for pc boards is rated for high-power applications. The Series 66 barrier-terminal strips are rated for voltages to 600V and currents up to 45A. They have a 0.5-in. terminal spacing and mount directly on a pc board. According to the company, the tri-barrier terminal strips provide significant space and installation cost savings over DIN-rail-mounted terminal blocks and bus bars. The terminal strips are available in sizes from two to 12 circuits and accept wires from 8 to 18 AWG. They cost $0.50 per circuit (1000). **Beau Interconnect Systems, Division of Vernitron Corp**, Laconia, NH. (603) 524-5101. **Circle No. 361**

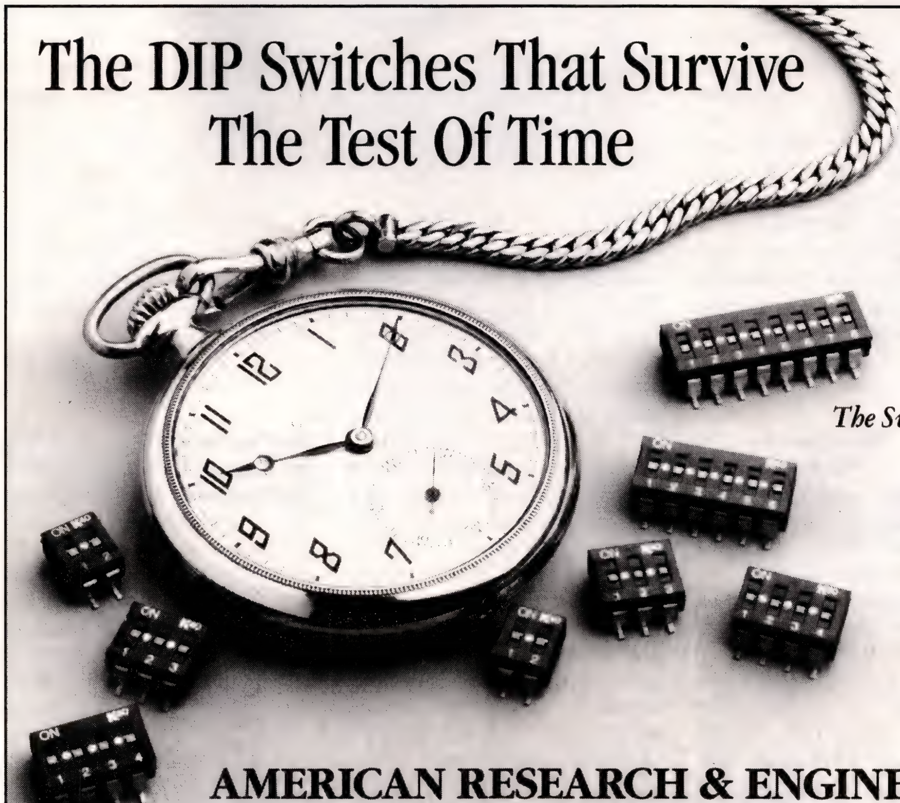
Halogen-lamp sockets operate to 250°C. The HT series halogen-lamp sockets are made from ceramic and mica with Teflon- and fiberglass-insulated lead wire. The high-temperature sockets hold all standard halogen lamps with MR-11, MR-16, G-4, and G-6.35 configurations. The sockets measure 17 mm in diameter and 9 mm deep. Lead wires are available in lengths to 220 mm. Maximum ratings are 250V and 250W. They cost from $0.69 to $1.69, depending on type and quantity. **Gilway Technical Lamp**, Woburn, MA. (617) 935-4442. **Circle No. 362**

Low-cost heat spreaders attach with pressure-sensitive adhesive. The T-Wing laminated heat spreaders cost from $0.50 to $1, depending on size and quantity. They are made from 5-oz copper with a 0.0015-in.-thick black film laminated to both sides for electrical insulation. Total thickness is less than 0.015 in. The compliant nature of these heat spreaders permits nearly 100% adhesive contact with a 5-psi application force, even on concave or otherwise nonflat package surfaces. **Chomerics Division of Parker Hannifin**, Woburn, MA. (617) 935-4850. **Circle No. 363**

Pin-grid-array socket for the NexGen Nx586 and NxVL system-logic devices. The PZA-463H-011A-37AT-F for the Nx586 µP costs $9.67 (5000). The PZA-401H011A-37AG-F for the NxVL device costs $8.38 (5000). Both sockets use ultra-low-insertion-force contacts. **McKenzie Technology**, Fremont, CA. (510) 651-2700. **Circle No. 364**

20-slot VME backplane has reduced crosstalk. The Model 910-6MO201-000 J1/J2 monolithic backplane has near-end crosstalk of <2% avg and peak-forward crosstalk of <5%. Testing was in accordance with Motorola's VME-backplane test specifications, using a 600-psec rise-time signal. Loaded backplane impedance is 50 to 65Ω with an average impedance of 55Ω. The backplane has a guaranteed impedance of 50Ω or greater. $858.38 (25). **Hadco Corp, Backplane Division**, Salem, NH. (603) 898-8010. **Circle No. 365**

Surface-mount LEDs. The SM110 series of LEDs is available in three high-efficiency colors: 635-nm red, 585-nm yellow, and 565-nm green. Also available are bicolor LEDs that provide a luminous intensity of 10 to 15 mcd from a 20-mA current. Package size is 4.5 mm high×4.5 mm across, and dome height is 3 mm. $0.44 (1000). **Ledtronics Inc**, Torrance, CA. (310) 534-1505. **Circle No. 366**



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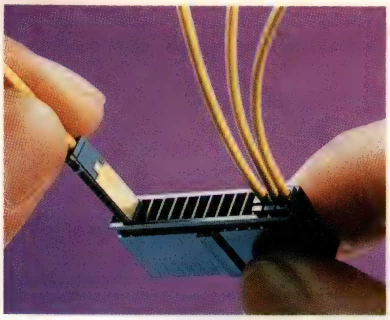

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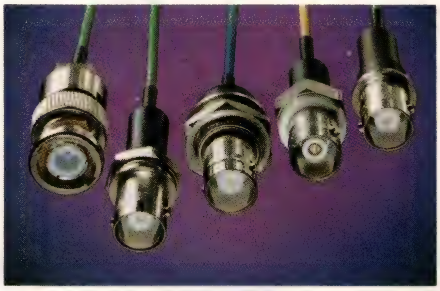

Meritec's impedance matched BNC cable assemblies feature precision, high strength molded terminations for high reliability in critical applications. The assemblies are available in a variety of configurations, including cable end plug, cable end jack, front panel mount jack with isolated ground and rear panel mount jack. The connectors are terminated to subminiature coax cable and feature standard BNC and cable impedances of 50 and 75 ohms. The assemblies may be terminated on the opposite end with Meritec SSI™, SSC™, GPI™ or PCB Soldertail Contact Interconnects. For specifications of BNC Terminations, see page 7 in our .100" Pitch SSI catalog.

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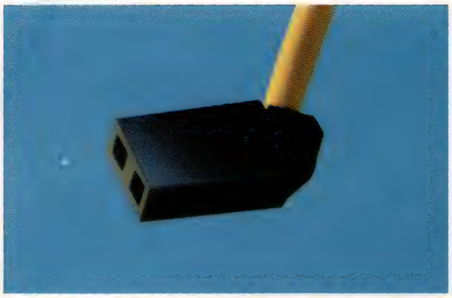

Meritec's low profile right angle GPI assemblies are engineered to meet critical space requirements. A minimum height clearance of 0.5 in. above the PCB minimizes the space needed to route cables. The GPI ground plane reduces crosstalk and controls the impedance mismatch through the connector, eliminating reflections at the termination. The assemblies are available in 50 and 75 ohm impedance for use in both high speed digital and critical analog signal applications. Detailed ordering information is on page 4 of our .100" Pitch SSI catalog.

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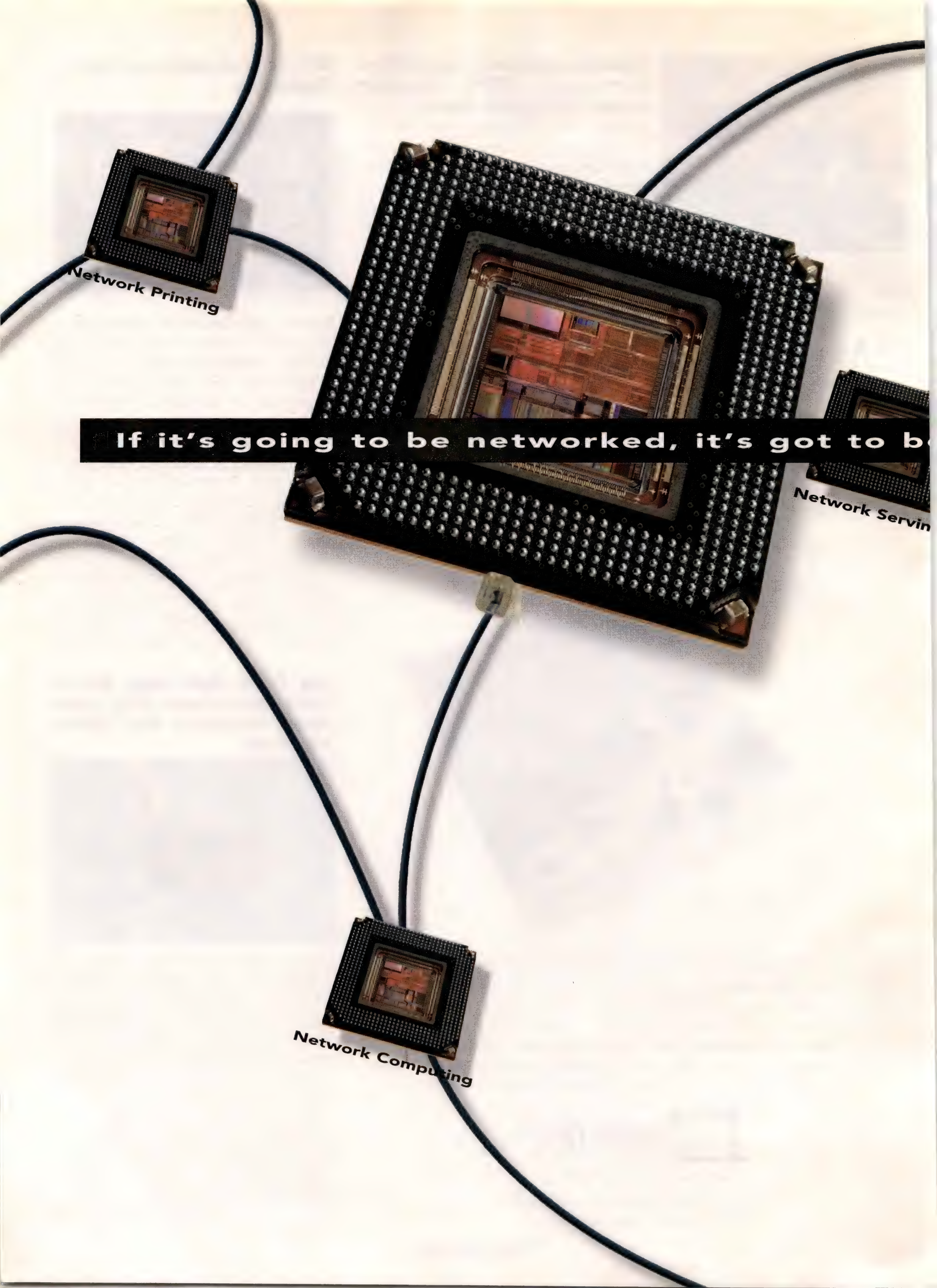
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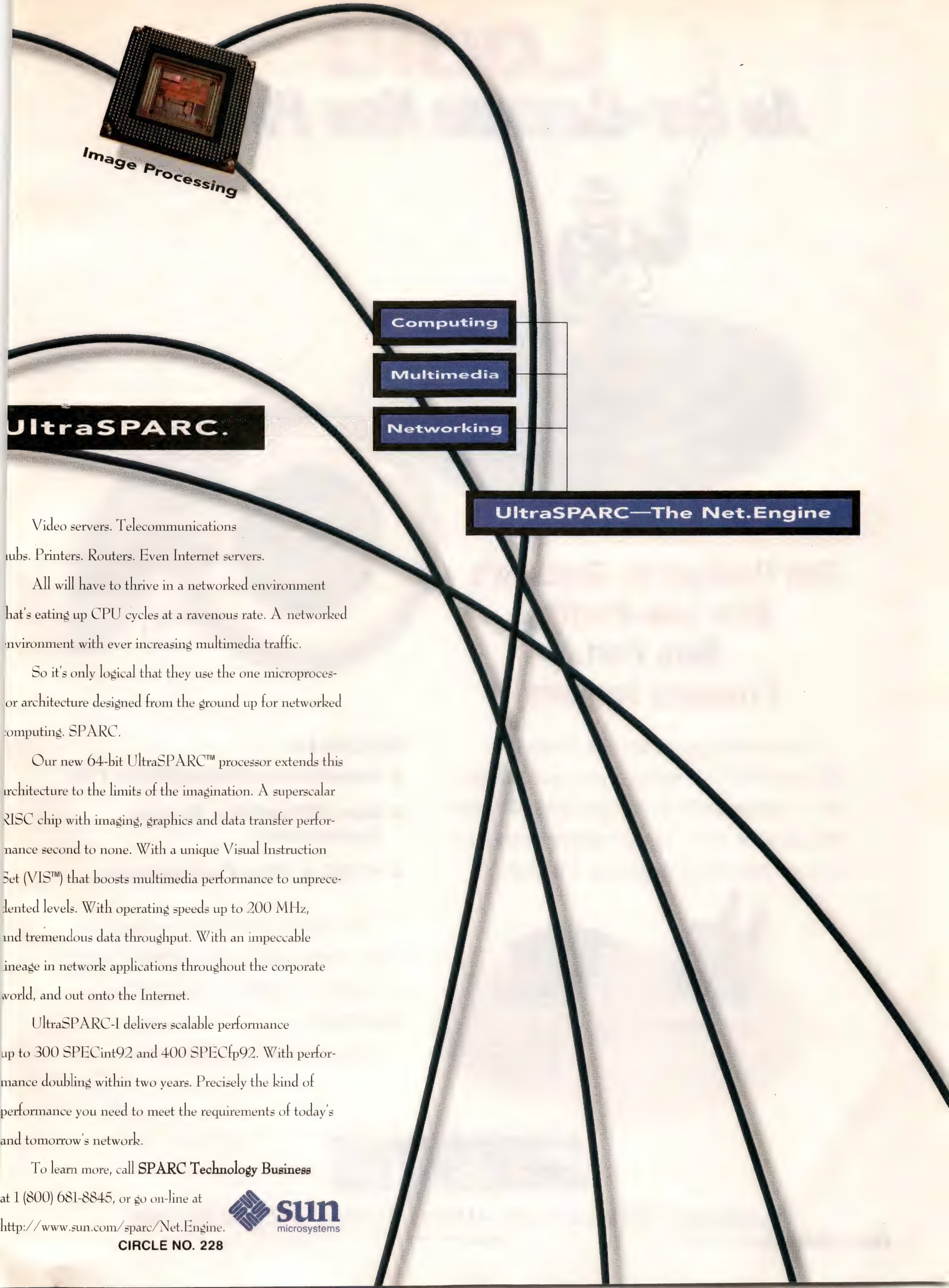

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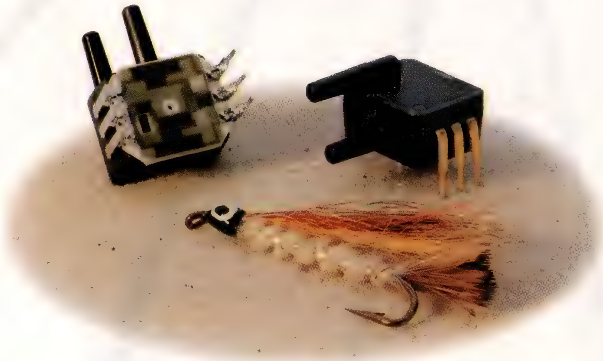

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Prolog for Macintosh, Unix, and DOS. Bell Northern Research (BNR) Ltd has licensed Applied Logic Systems (ALS) to merge the ALS Prolog compiler system with BNR Prolog. Version 3.5 of BNR Prolog costs <$100. Other versions for Unix and DOS are also available. **Applied Logic Systems Inc**, Newton Centre, MA. (617) 965-9191. **Circle No. 368**

DEC Alpha compilers for NDP Fortran, C/C++, and NDP Pascal. The compilers run under Windows NT and OSF and require the use of the Digital Equipment Corp Alpha assembler and the appropriate system linker. The NDP family of compilers uses a vectorizing scheduler to maximize Alpha throughput for high performance. The Windows NT versions of the compilers cost $795. **Microway**, Kingston, MA. (508) 746-7341.
Circle No. 369

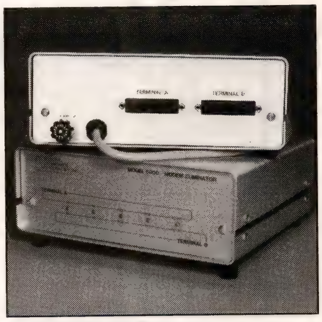
▲Learn to design with FPGAs. The epXkit combines epXboard with the 240-pg "FPGA Workout." The text illustrates how to design combinatorial logic, counters, state machines, and a 4-bit μC, using field-programmable gate arrays (FPGAs). The epXboard is based on the Altera EPX780 FPGA and has the equivalent of 3500 gates. The PLDshell programming tool lets you describe your logic with Boolean equations, truth tables, or state-transition statements. A graphical simulator lets you check your design before loading it into the pc board through a PC's printer port. The FPGA uses static RAM, letting you quickly modify designs. The kit costs $169.95. **Xess Corp**, Apex, NC. (919) 387-1302.
Circle No. 370

486 PC system board integrates graphics, sound, fax, and LAN. The LPM30 supports 64-bit accelerated local-bus graphics, 16-bit stereo sound, enhanced IDE CD-ROM drives, voice/fax/data modems, and twisted-pair Ethernet. The board lets system integrators and resellers create multimedia systems that do not require add-in cards. Integrating these functions on the system board saves money and avoids DMA and interrupt-request conflicts. The board accommodates a variety of 3.3, 4, and 5V, 486-class processors from Advanced Micro Devices, Cyrix, and Intel. The board without modem and LAN options costs $275 (OEM), including a 128-kbyte cache memory and 1-Mbyte video memory. **Micronics Computers Inc**, Fremont, CA. (800) 577-0977.
Circle No. 371

3.5-in. hard-disk drives suit high-throughput, uninterrupted data transfers. The Quantum Trailblazer drives offer 420- ($215) and 850-Mbyte ($315) capacities. They operate at 4500 rpm and have a 14-msec average seek time. MTBF is 300,000 hours. The 540- ($240) and 1080-Mbyte ($395) Fireball drives have an MTBF of 500,000 hours. Both drive families use the company's AutoTransfer technology to minimize command overhead and Multiple AutoRead and Multiple AutoWrite ASICs to improve sequential data transfers. The drives use an embedded-servo scheme, which intersperses positioning information with user data on each disk. The embedded-servo scheme eliminates the need for the thermal recalibrations that other servo methods require. Thermal recalibrations sometimes result in delays that cause missed frames in movies or noticeable gaps in music. The drives feature a Fast ATA-2 interface for data transfers as fast as 16.6 Mbytes/sec. The Fireball drives also support Fast SCSI-3 data transfers of up to 10 Mbytes/sec. **Quantum Corp**, Milpitas, CA. (408) 894-4000.
Circle No. 372

C library available as DLL for PCs running under Windows 3.1. The C library dynamic-link library (DLL) suits software developers, scientists, and engineers who need to integrate numerical C routines into their Windows programs and applications. Your software can call and load the routines at runtime from within Windows programs. The library includes >250 routines, providing functions for minimization, ordinary differential equations, Fourier transforms, quadrature, linear algebra, solutions of systems, curve and surface fitting, special functions, statistical functions, and other numerical computations. You can seamlessly integrate the DLLs with C/C++ Windows software, and you can call the DLLs from Visual Basic and integrate them with Windows applications, such as Excel. $495. **Numerical Algorithms Group Inc**, Downers Grove, IL. (708) 971-2337.
Circle No. 373

Double-speed CD records and plays back. The Deltix CD-R2 for audio-recording and premastering applications supports most multimedia and interactive-CD data formats, including CD-DA, CD-ROM, CD-ROM XA, CD-I, and Photo CD. The unit comes with a SCSI-2 interface, SCSI cards, SCSI cables, media, audio jacks, a power cord, a caddie, and software. Prices for subsystems for Macintosh- or Windows-based systems start at $1795. **Olympus Image System Inc**, Woodbury, NY. (516) 364-3000.
Circle No. 374



Synchronous modem eliminator allows direct connection between terminals and computers. The Model 5000 synchronous modem eliminator regenerates data and clock signals, extending the allowable distance between computer and terminals to 100 ft. Low-capacitance cables extend the connection distance to 500 ft. Internal switch settings allow data rate selection from 1200 to 19,200 bps and request-to-send/clear-to-send delay selection from 0 to 150 msec. The unit's crystal-controlled oscillator or either terminal device supplies timing. Five LEDs provide status of data, timing, and handshake signals for both terminals. The unit costs $350. **Electro Standards Laboratory Inc**, Cranston, RI. (401) 943-1164. **Circle No. 375**

Tape-backup units for Windows NT systems. The MS4000DATx—NT is based on a SCSI DDS/DC digital-audio-tape (DAT) drive and offers 4 Gbytes of storage capacity when using hardware data compression. Native-mode transfer speed is 22 Mbytes/minute, and compressed-mode transfer speed is 44 Mbytes/minute. An internal version of the unit costs $1995, and an external version costs $2195. The MS8000-DATx—NT is based on a SCSI DDS-2 DAT drive and offers up to 8 Gbytes of storage capacity with a 48-Mbyte/minute data-transfer rate. Bit-error rate is <1 in 10^{15}. MTBF exceeds 150,000 hours. An internal version of the unit costs $2395, and an external version costs $2595. **Conner Peripherals Inc, Tape Products Group**, Costa Mesa, CA. (714) 641-1230.

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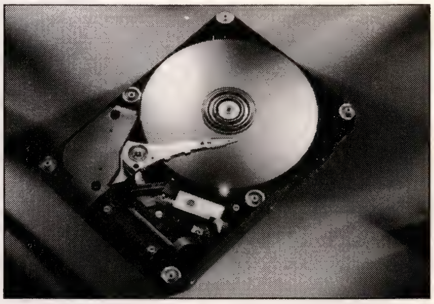
3.5-in. disk-drive families offer 2.1- to 9.1-Gbyte capacities. The 5400-rpm Empire II family and the 7200-rpm Atlas II families use partial-response/maximum-likelihood read channels and magnetoresistive heads. Specifications for the Empire II drives include an 8.9-msec seek time, a 90-Mbps read-channel data rate, and a 40-Mbyte/sec external data rate. Specifications for the Atlas II drives include a 7.9-msec seek time, a 110-Mbps read-channel data rate, and a 200-Mbyte/sec external data rate. The 2.1- and 4.3-Gbyte drives are 1 in. high, and the 9.1-Gbyte drives are 1.63 in. high. MTBF is 1 million hours. Prices for the Empire II drives range from $995 to $2495, and prices for the Atlas II drives range from $1195 to $2995. **Quantum Corp**, Milpitas, CA. (408) 894-4000.



Circle No. 377

Color VGA LCD kit lets you evaluate color LCDs for $995. The Color VGA LCD Simplicity Kit includes a 9.4-in. color display with 4096 colors, cold-cathode fluorescent-tube backlighting, a 16-bit ISA bus-controller card, a backlight inverter, and cables. An optional analog touchscreen provides up to 1024 touch points. **Apollo Display Technology Inc**, Holtsville, NY. (516) 654-1143. **Circle No. 378**

Frame grabber is compatible with a wide variety of video sources. The Imascan/Precision Peripheral Component Interconnect (PCI)/VL bus board works with color or monochrome video sources, including National TV Systems Committee/phase-alternation line standards, S-

Faster than an analog scope. And with instant replay.

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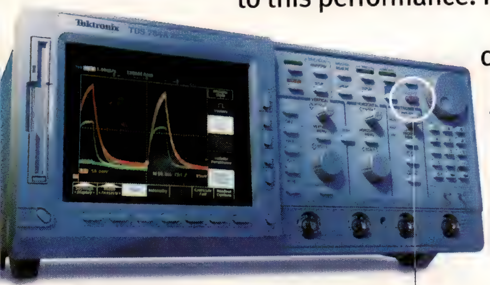

The TDS 700A series gives you true representation of signals, with up to 1 GHz bandwidth and a 4 GS/s sample rate. Plus, it's got the same familiar interface as the entire TDS line so you won't have to learn anything new.

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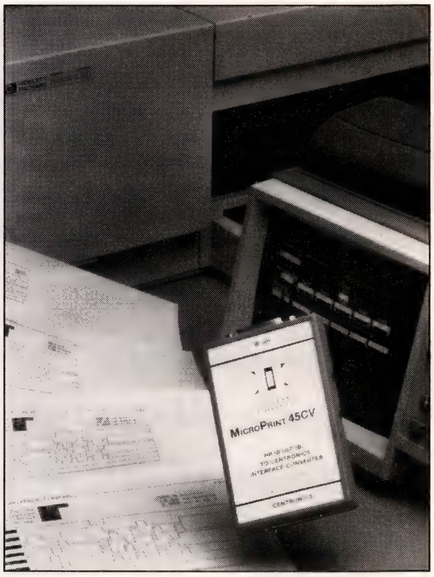
CIRCLE NO. 102

Video, RS-170/Consultative Committee, International Radio, and RGB/YUV. Color sources are digitized to 24-bit accuracy, and monochrome sources are digitized to 8-bit accuracy. The board offers a variety of features to ensure high precision in the video captures. Sub-pixel clock adjustment provides exact pixel centering. You can synchronize video captures with an external trigger. The board, including drivers for imaging application software, costs $1595. **Imagraph Corp**, Chelmsford, MA. (508) 256-4624. **Circle No. 379**

Rack-mount SCSI switch lets you share 32 SCSI devices between two computers. The SCSI Switch, a 4×2 electronic crosspoint switch, provides transparent selection of up to 32 SCSI devices between two computer systems. You can control the unit from the front panel or via a remote RS-232C interface. The system supports 10-Mbyte/sec data rates on 8-bit (narrow) versions and 20-Mbyte/sec Fast SCSI devices on 16-bit (wide) versions. Six models costs $1545 to $2245. **Applied Concepts Inc**, Wilsonville, OR. (503) 685-9300. **Circle No. 380**

IEEE-488 converter automatically sizes graphics and lets you substitute HP printers for plotters. The MicroPrint 45CV converts IEEE-488 to Centronics and connects to HP Centronics printers, HP computers, and automatic-test-equipment (ATE) systems with IEEE-488 interfaces. The unit is transparent to ATE software and requires no software changes or additions. The device solves the problem HP printers cause by defaulting to their lowest or highest resolution on power-up. An HP-GL mode lets you use HP LaserJet, ThinkJet, PaintJet, QuietJet, and DeskJet printers instead of plotters. The device costs $299. **Intelligent Interfaces Inc**, Stone Mountain, GA. (404) 381-9891. **Circle No. 381**



Digital-audio board for ISA bus supports apt-X encoding and other compression formats. The SX-26 digital-audio board also supports ISO/MPEG-1 Layer I/II, Dolby AC-2, Oki adaptive differential PCM (ADPCM), Microsoft ADPCM, DVI ADPCM, CDI ADPCM, CD-ROM XA, and 8- and 16-bit PCM. The board uses the TMS320C31 DSP and can simulta-

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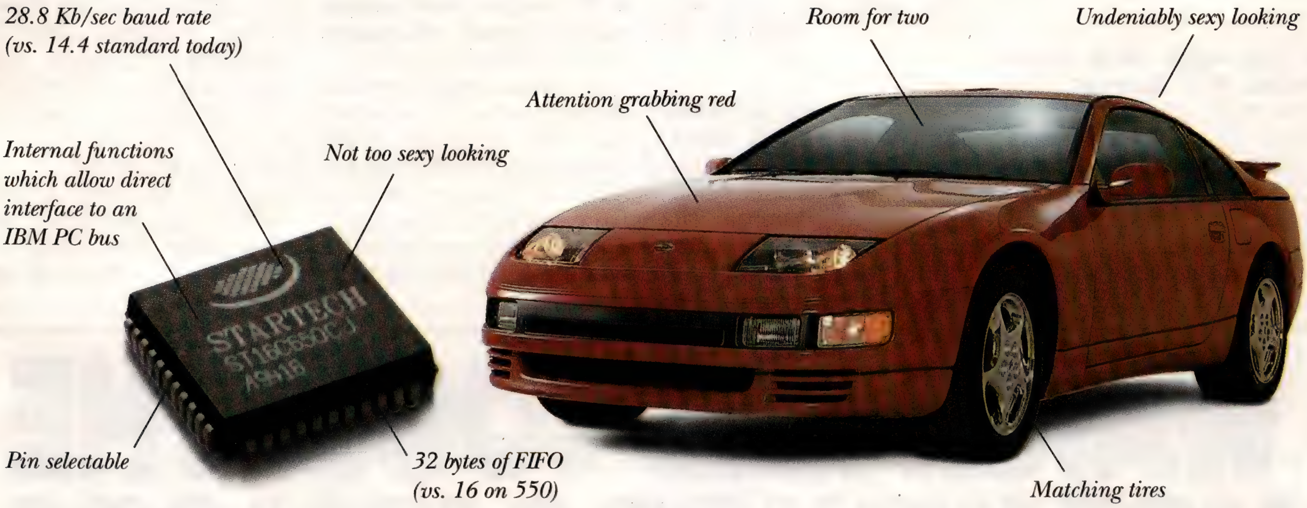
CIRCLE NO. 34

Both are turbos with a V6 engine, but the one on the left will launch the next generation of modem devices.



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CIRCLE NO. 104

neously record or play two independent stereo digital-audio files. The board also provides balanced and unbalanced analog and AES/EBU or S/PDIF digital input and output for maintaining the integrity of the original analog or digital signal. The board includes software drivers for Windows, Windows NT, and DOS. The board costs $3495. An audio developer's kit supporting C, Pascal, and Basic costs $750. **Antex Electronics Corp**, Gardena, CA. (310) 532-3092. **Circle No. 382**

0.5-in.-high disk drive holds 815 Mbytes. The MK-1926F 2.5-in. disk drive has a 13-msec average seek time and weighs 150g. The three-platter drive has an internal 44.9-Mbps data-transfer rate, a 128-kbyte cache buffer, and a 4200-rpm spin speed. It draws 1W from a 5V supply and has a 5-sec spin-up time. The drive is available with a Fast ATbus-attachment (ATA) or SCSI-2 interface. With a SCSI-2 interface, the drive has a 10-Mbyte/sec synchronous data-transfer rate and a 6-Mbyte/sec asynchronous data-transfer rate. The Fast ATA interface supports multiword DMA mode 2 and PIO mode 4 data transfers at 16.6 Mbytes/sec. Samples cost $1000. **Toshiba America Information Systems Inc, Disk Products Division**, Irvine, CA. (714) 457-0777. **Circle No. 383**

Disk drive series adds Fast/Wide SCSI-2 interface. The AV Gold Series disk drives now offer a minimum sustained transfer rate of 4 Mbytes/sec with a maximum burst rate of 20 Mbytes/sec. The series includes the $3950, 5.25-in. Scorpio 9 Model 199WAV with a 9.1-Gbyte formatted capacity; the $2510, 3.5-in. Capricorn 4 model 3243-WAV with a 4.3-Gbyte capacity; and the $1950 Taurus 2 model 4221WAV with a 2.1-Gbyte capacity. The drives have a 650,000-hour MTBF. **Micropolis Corp**, Chatsworth, CA. (818) 709-3300. **Circle No. 384**

Remote-access system integrates 16-port switch, V.34 modem, and a time-synchronized password. The ISAS-7016 integrated secure-access system provides secure access for networks and other computer devices using the SecureID card and ACM-100 access module from Security Dynamics. The SecureID card provides two levels of authorization based on passwords that change every 60 sec. Passwords are time-synchronized with the ACM units. The system operates from 110V ac or 48V dc and costs $2899. **Gilltro-Electronics Inc**, Santa Clara, CA. (408) 727-6422. **Circle No. 385**

TFT, 9.4-in., active-matrix, color LCD is rack-mountable. The thin-film-transistor (TFT) RMM280 LCD includes rack mounting. Standard VGA output drives the 640×480-pixel-resolution, 4096-color LCD. Front-panel controls include brightness, contrast, VGA text, tracking, frequency, vertical, and horizontal positioning. The monitor measures 19 in. wide×8.75 in. high×5.5 in. deep. It costs $2995 (10). **Recortec Inc**, Sunnyvale, CA. (408) 734-1290. **Circle No. 386**

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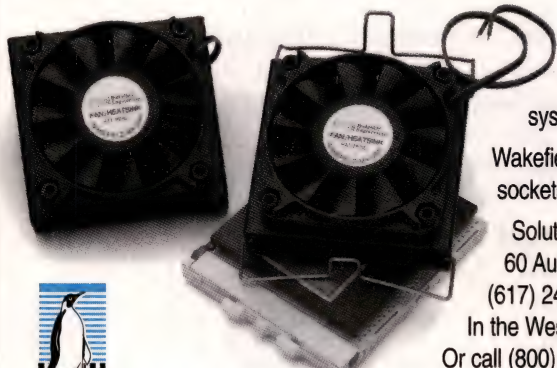

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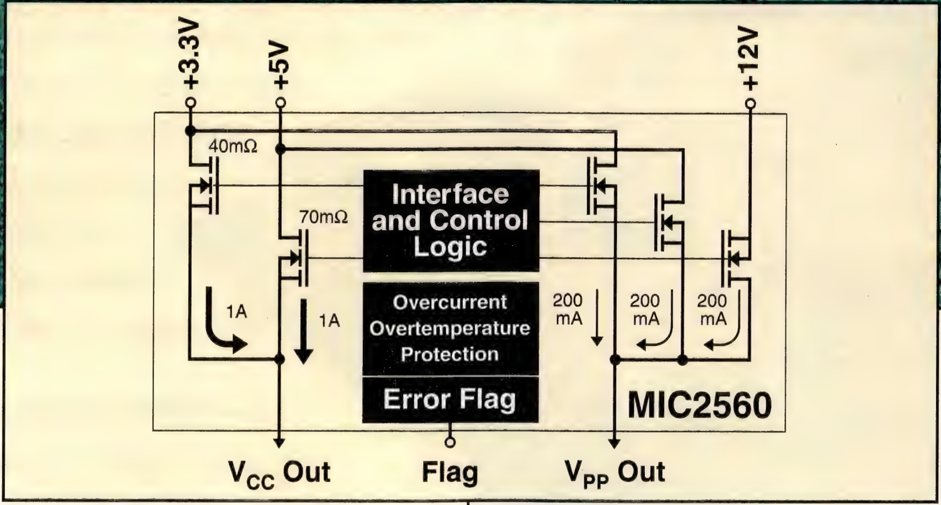

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- On-chip thermal sense and overload shutdown
- Flag output for over current or over temperature conditions
- Controlled rise and fall times
- Built-in illegal-state lockout control eliminates switch "shoot through"

Micrel PCMCIA Switching Products	Availability
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MIC2558 Dual V_{PP} Switch Matrix	Available Now
MIC2560 V_{CC} & V_{PP} Power Controller with Full Protection	Available Now
MIC2561 Low Cost V_{CC} & V_{PP} Switch Matrix with Full Protection	Available Now

Designed For System Compatibility

The MIC2560 is designed to exceed the latest and most stringent PCMCIA specifications and recommendations. It can output one amp V_{CC} current at either 3.3V or 5V with insignificant loss across its 40 milliohm switch and provides a V_{PP} output of 200 milliamps at all standard voltage levels. The MIC2560 is available in versions that interface with most of the popular PCMCIA logic controllers on the market today! And if your application doesn't require the ultra low on resistance of the MIC2560, the new MIC2561 offers the same features but at a reduced price.

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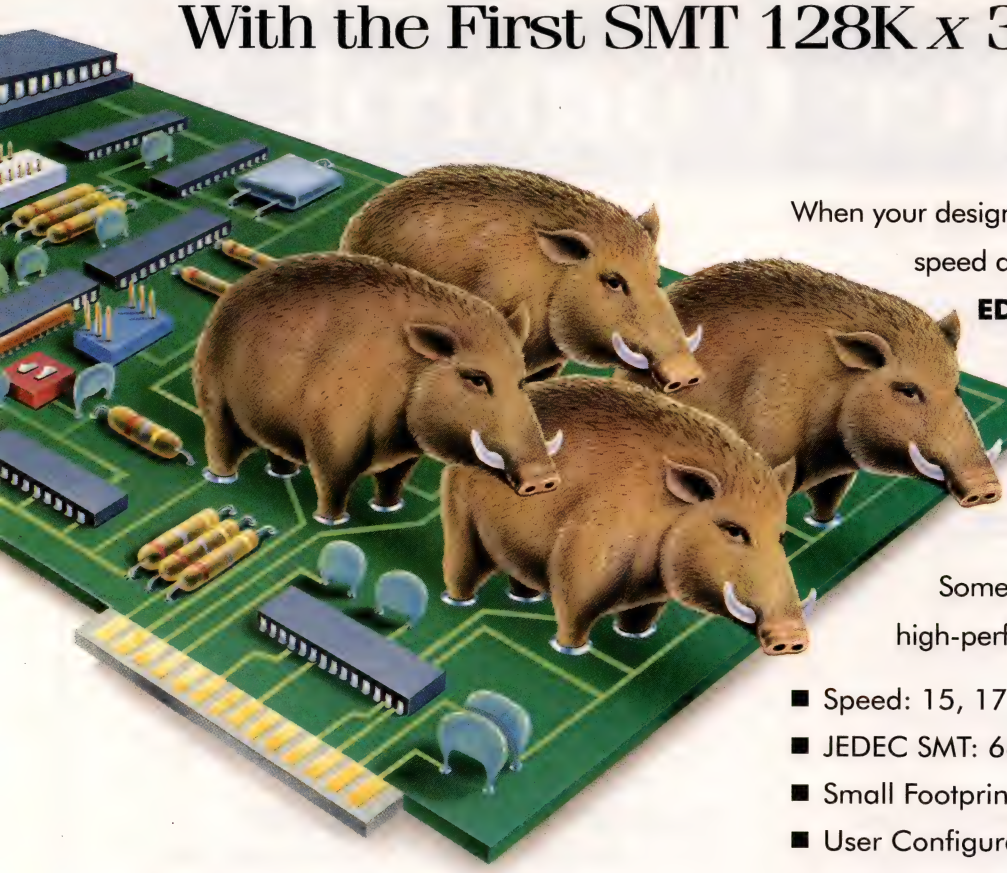

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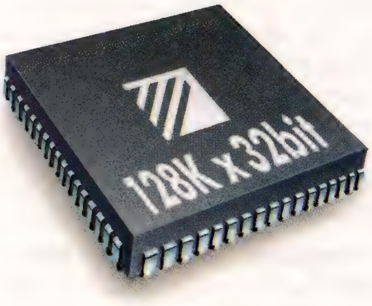

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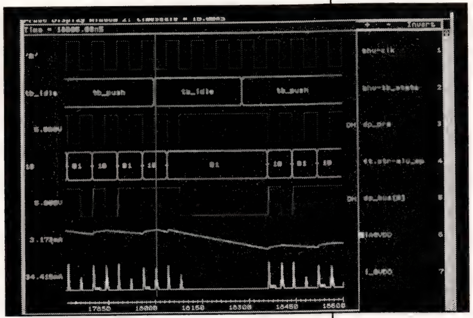
Native-compiled-code simulator speeds execution. The NC-Verilog simulator uses the company's Interleaved Native Compiled-code Architecture (INCA) to provide a speed increase over Verilog-XL Turbo at the register-transfer level. The simulator also uses memory more efficiently. According to the company, the new architecture will eventually allow multiple types of simulation, such as Verilog, VHDL, event-driven, cycle-based, digital, and analog, to execute concurrently without co-simulation penalties. NC-Verilog will go into beta testing in the second quarter of this year. The company plans to begin shipments this year. From $32,000. **Cadence Design Systems Inc**, San Jose, CA. (408) 943-1234.
Circle No. 342

Software converts pc-board graphic formats for viewing and printing under Windows. CAMCAD for Windows lets you view, print, compose, and convert pc-board graphics formats including Gerber, HPGL, and DXF. The software lets you view conversions before printing to verify correct layer assignments and other features. The CAMCAD viewer costs $200. Options start at $99 for the Gerber/DXF/HPGL view and print module. **Router Solutions Inc**, Newport Beach, CA. (714) 721-1017.
Circle No. 343

New release of Verilog simulator doubles previous performance. The Verilog Compiled Simulator (VCS) 3.0 has new optimization features that improve performance, regardless of which Verilog constructs you use. The simulator makes the greatest improvements in large designs. According to the company, a processor design that took 75 sec to run on the earlier version of VCS takes 37 sec on the new version. The simulator is available immediately and costs $40,000 for a floating license. **Chronologic Simulation**, Los Altos, CA. (415) 965-3312.
Circle No. 344

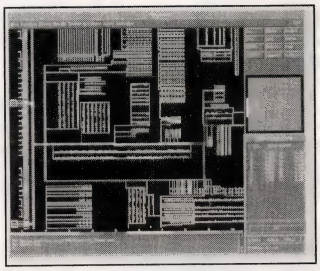
Kit converts gate-arrays into FPGAs. The Altera gate-array conversion kit lets you convert gate arrays to field-programmable gate arrays (FPGAs). According to the company, gate-array vendors are phasing out some gate-array designs using old process technology as the vendors migrate to new submicron processes. The free conversion kit provides a way to keep those designs in production using the company's programmable logic. The kit supports LSI Logic's LCA100K, LCA-200K, and LCA300K families and Fujitsu's CG24 library. Translation for other vendors is in progress. **Altera Corp**, San Jose, CA. (408) 894-7000. **Circle No. 345**



⬆Signal-integrity tool simulates the effects of nonideal power and ground planes. Contec-Delta-I combines a pc-board- and multichip-module (MCM)-layout interface with a 3-D inductance and resistance field solver. The tool simulates the effects of imperfect reference planes on the operation of traces and discrete components. The software reads the geometries of the planes and their discontinuities directly from layout programs. The signal-integrity tool currently supports Cadence Allegro, Mentor Graphics Board Station and MCM Station, and Zuken-Redac tools. It runs on HP Series 700 and Sun SPARCstation workstations. The tool costs $30,000 for a fixed-node license and $36,000 for a floating-node network license. **Contec Microelectronics USA Inc**, San Jose, CA. (408) 434-6767. **Circle No. 346**

PLD tool adds Verilog simulator. The Synario Windows-based design tool for programmable logic offers integration with FrontLine Design Automation's BaseLine Verilog simulator. The Verilog XL-compatible simulator is available in two options. The first option costs $2995 and provides entry-level simulation support, a subset of BaseLine's simulation capabilities. The second option costs $4995 and includes additional functions, such as source-level debugging and Programming Language Interface support. **Data I/O**, Redmond, WA. (206) 881-6444.
Circle No. 347

Synthesizable SONET core for asynchronous-transfer mode. The synchronous-optical-network (SONET) User Network Interface processor core implements transmission convergence and cell delineation with a Utopia interface. You can synthesize the core by using Synopsys and field-programmable gate-array synthesis tools. End users can license the product, and ASIC vendors can add the core to their libraries. Prices for the gate-level design and source code begin at $120,000. VHDL versions cost extra, depending on the VHDL simulator you use. **AdvanCell Logic Corp**, Cupertino, CA. (408) 777-9915. **Circle No. 348**



IC-analysis software detects electromigration and voltage-drop problems. RailMill helps you analyze complex, high-performance, deep-submicron designs. The tool analyzes current and voltage behavior and indicates where local current density or voltage drop is likely to cause failure and reduce product lifetime. Prices for the tool start at $130,000. **Epic Design Technology**, Santa Clara, CA. (408) 988-2997.
Circle No. 349

Electronic-design-entry and -analysis tool runs under Windows. Spice-It for Windows provides a schematic editor, an interactive graphical simulation engine, libraries, and a device and symbol editor. The system lets you model and analyze digital, analog, and nonelectronic systems at multiple levels of abstraction. The software costs $1895. Spice-It for Windows NT costs $2095. Both will be available in the second quarter. **CAD-Migos Software Tools Inc**, Redwood City, CA. (415) 369-5853.
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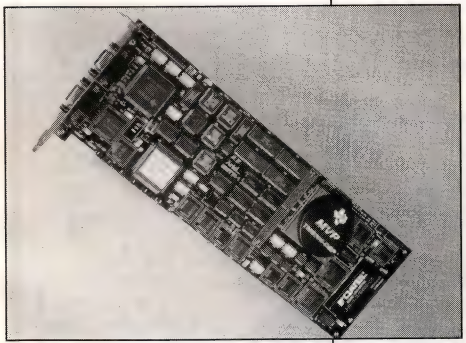
24-Mbyte solid-state disk board for PC/104. The Promdisk V-104 solid-state disk-emulator board emulates one or two bootable read/write fixed-disk drives with capacities of 1 to 24 Mbytes using flash memory. The board includes a BIOS-extension ROM, which contains the Datalight FTL integrated flash file system and boot utilities. The board is compatible with DOS and Windows, letting you copy, read, and erase files using standard DOS commands. The solid-state disk drive suits harsh environments and provides the additional benefits of smaller size, lighter weight, lower power consumption, and higher speed than do mechanical disk drives. Prices start at $119 for a 1-Mbyte board. **Micro Computer Specialists Inc**, Vista, CA. (619) 598-2177. **Circle No. 326**



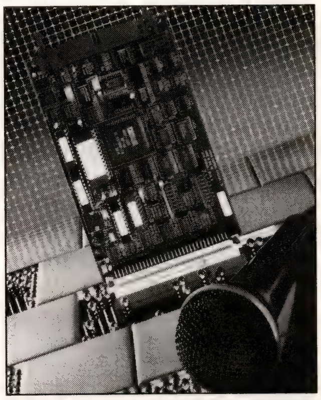
▲PCI bus board has TMS320C80 DSP and high-resolution graphics. The Griffin has a full 32-bit master/slave PCI bus interface, up to 8 Mbytes of DRAM, and a 24-bit RGB graphics interface with a 4-Mbyte video-RAM frame buffer. For memory expansion, I/O, and other peripheral options, the board provides a stackable mezzanine-bus interface providing direct access to the TMS320-C80's key signals. A 512×32-bit synchronous bidirectional FIFO buffer accommodates data streaming between the C80 DSP and the PCI bus interface. A 4k×32-bit dual-port RAM also links the C80 and PCI bus. The video output is based on the TVP3025 RAMDAC and provides resolutions up to 1600×1280 pixels at 16 bits/pixel or 1024×768 pixels at 24 bits/pixel. The board will be available in the third quarter for $8995. **Ariel Corp**, Highland Park, NJ. (908) 249-2900. **Circle No. 327**

RTOS supports Motorola's 68302 communications processor. The RTXC real-time operating system (RTOS), a multitasking, real-time executive, lets you develop a small, fast, ROMable RTOS for your application. When combined with Windows-licensed SingleStep from Software Development Systems, the RTOS provides a seamless development and debugging environment. The tools provide full source-level simulation, access to all program objects, kernel awareness during debugging, and integration with an ANSI C/C++ compiler. The royalty-free RTOS includes source code. V3.2 starts at $1495. **Embedded Systems Products Inc**, Houston, TX. (713) 728-9688. **Circle No. 328**

Development kit for systems integrating the Access.bus and smart power-management devices. The Access.bus system-management development kit (SMDK) is a PC-based environment for the design, development, and testing of system-management (SM) bus devices, software drivers, and applications. The release of SMDK corresponds with the expansion of the Access.bus specification to accommodate Intel's SMbus. The combined specification defines a unified software architecture for a single controller that accommodates internal SM-bus devices and external Access.bus peripherals. The SMDK costs $2750. **Computer Access Technology Corp**, Santa Clara, CA. (408) 727-6600. **Circle No. 329**

Telephony libraries for Analog Devices' DSPs. The Telephony Libraries are compatible with Analog Devices' ADSP21xx fixed-point DSPs and ADSP21k floating-point DSPs. The libraries include signal-processing functions, such as acoustical echo cancellation, DTMF tone generation/detection, call-progress monitoring, caller identification, AGC, and line-echo cancellation. All the functions are coded in assembly language and are callable by C programs. Each library costs $50,000 plus royalty. **GAO Research & Consulting Ltd**, Toronto, ON, Canada. (416) 292-0038. **Circle No. 330**

VMEbus-based embedded computer uses 486-DX2. The EPC-8 embedded computer uses a 50- or 66-MHz 486DX2. The board provides Ethernet, local-bus Super VGA graphics, a watchdog timer, optional flash memory, and optional battery-backed SRAM. I/O interfaces include an RS-232C port, an RS-422/485 port, a parallel printer port, and a PS/2-style keyboard interface. Expansion modules are available for a variety of I/O and mass-storage interfacing options. A 50-MHz board with 4 Mbytes of onboard DRAM costs $2247 (100), and a 66-MHz version costs $2397 (100). **Radisys Corp**, Beaverton, OR. (503) 646-1800. **Circle No. 331**

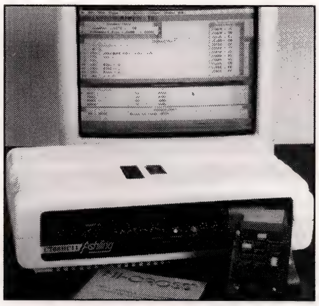


DSP-based STEbus board operates as intelligent data-acquisition and -control system. The Sadio board has a 16-bit SP2105 DSP, eight 12-bit multiplexed A/D channels, and two 12-bit DAC outputs. The device's 32 kbytes of dual-ported RAM link the board and the STEbus. The board also provides 12 16-bit timer/counters, three interrupt sources, and two byte-wide latches for generating TTL-level digital outputs. The board costs £575. **Arcom Control Systems Ltd**, Cambridge, UK. +44 (0)223 411200. **Circle No. 332**

Software-development tools for SuperH 32-bit RISC and H8 embedded controllers. The computer-aided real-time-design tools (CARDtools) let you design and implement application software using graphical tools. You can simulate applications before writing code, checking for missed time deadlines, memory usage, race conditions, and other timing-behavior problems. The software automatically generates ANSI C code and provides automatic documentation to ISO 9000 standards, including design traceability. The complete CARDtools set costs $25,000. **CARDtools Systems**, Sunnyvale, CA. (408) 559-4240. **Circle No. 333**

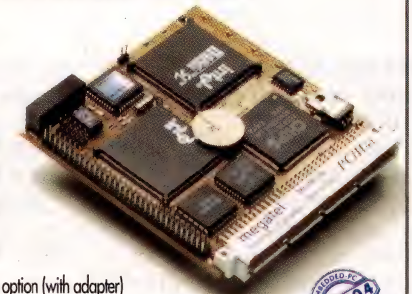
Development kit for real-mode 80x86 real-time applications. The VRTX x86/rm application-development kit provides development support for any 80x86-compatible processor, including Advanced Micro Devices' AM386EM; Intel's 386EX; and other 80386-, 80486-, and Pentium-compatible processors. The kit includes the VRTX x86/rm real-time operating system and a set of software-development tools, including the company's ANSI C compiler, a macro assembler, a linker/locator, and an object-module librarian. It also includes the company's Xray x86/rm source-level target-linked debugger. The kit costs $2500. A development license for the optional IFX x86/rm I/O and file-management module costs $495, the WIX x86/rm Window I/O module costs $349, and the Xray x86/rm instruction-set simulator costs $895. **Microtec Research Inc**, Santa Clara, CA. (408) 980-1300. **Circle No. 334**

Image-processing library for the TMS320C40 DSP. The EyeLib library provides building blocks for developers implementing standard image-processing routines. The library contains >400 functions covering operations such as fast edge detection, convolutions, 2-D FFTs, binarizing, filtering, and image enhancement. The routines are callable from C, C++, assembly, and Ada. The universal library runs on any board-level C40-based system under any software environment. It costs $5000. **Sinectonalysis Inc**, West Newton, MA. (617) 894-8296. **Circle No. 335**



Development systems provide real-time in-circuit emulation for 68HC11, HC08, and HC05. The CT68HC11 and CT68HC08 μP-development systems work with the Archimedes/Hiware Hi-Cross C compilers to let you customize display windows and single-step over C statements. The systems also support standard and user-defined data types and have a real-time trace system that displays a back-annotated trace of program execution in C without interrupting program execution. Prices for the development systems for the 68HC11 or 68HC08/05 start at $4350. **Ashling Microsystems/Eastern Systems Inc**, Westborough, MA. (508) 366-3220. **Circle No. 336**

PC-based image-processing system has frame grabber and uses TI C40 DSPs. The Spirit-Image for DSP and non-DSP programmers needing to perform hundreds to thousands of



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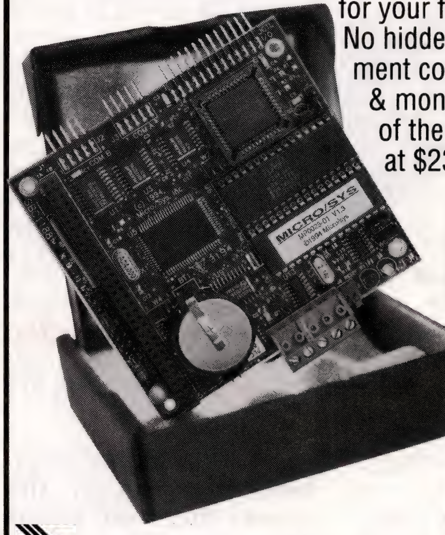

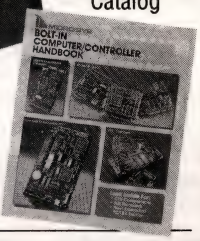

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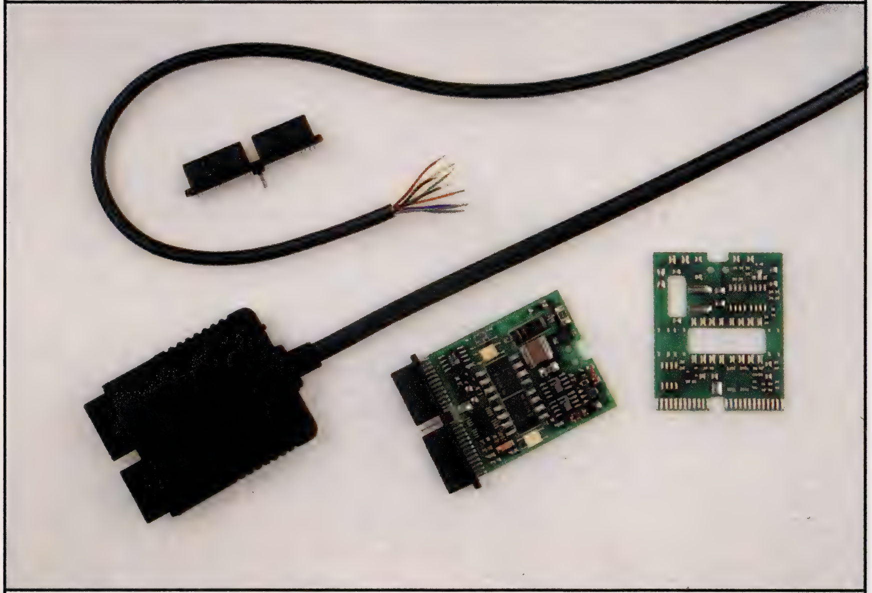

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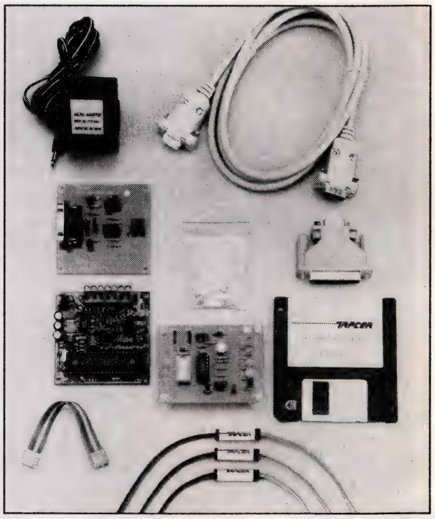

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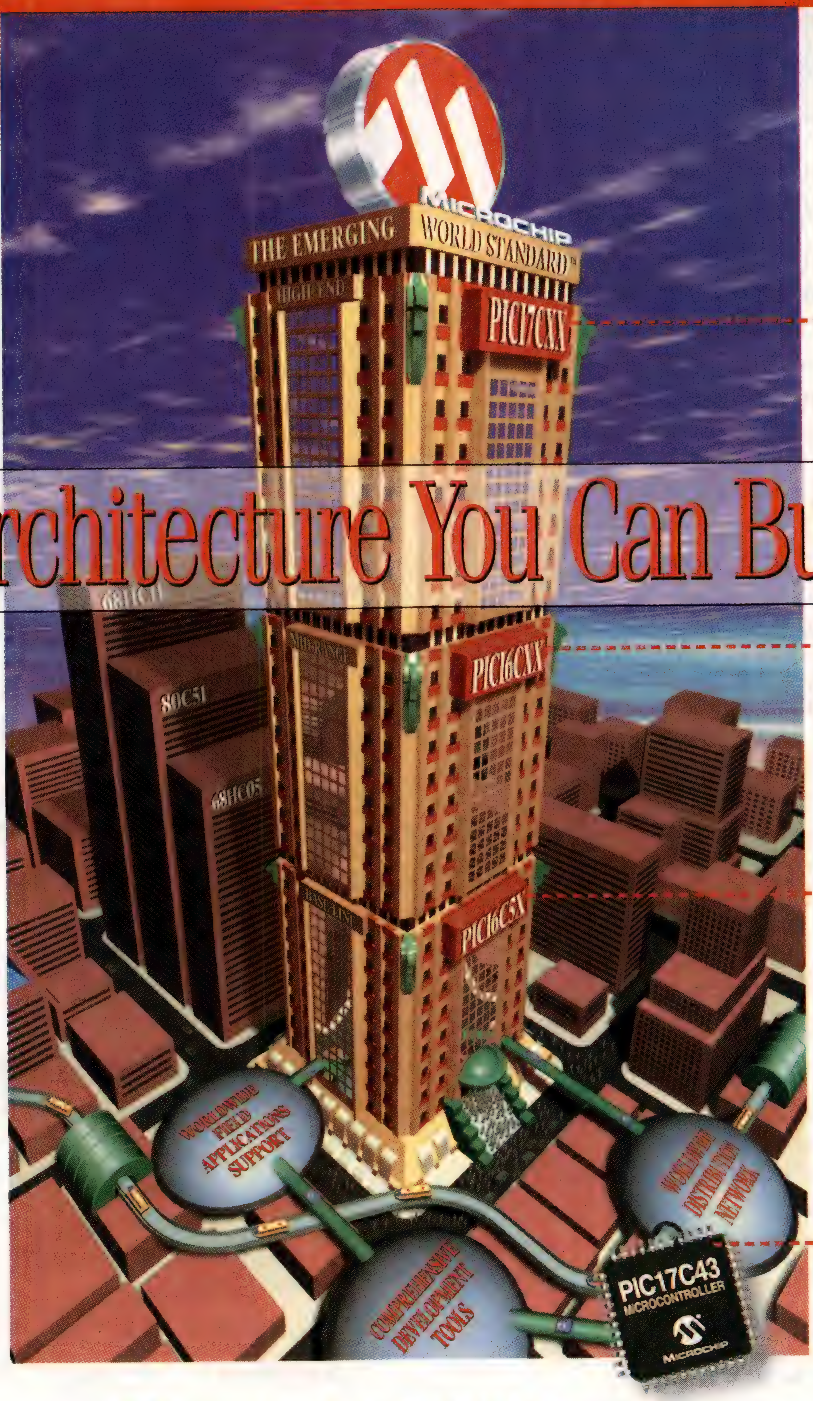
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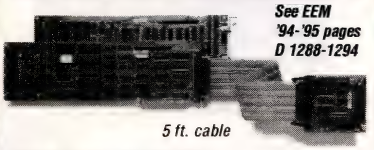

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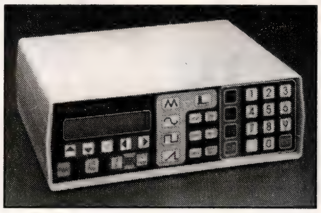

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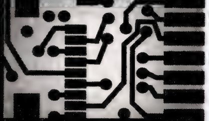

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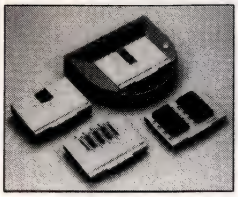

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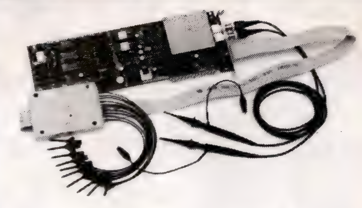

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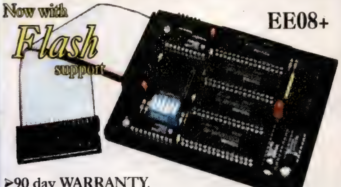

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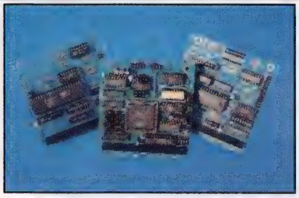

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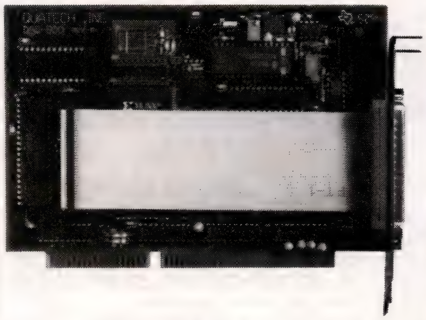

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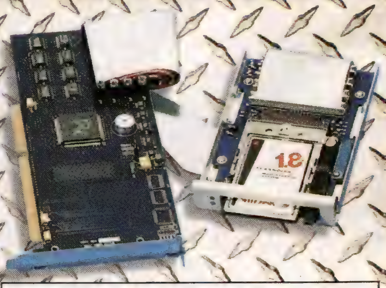

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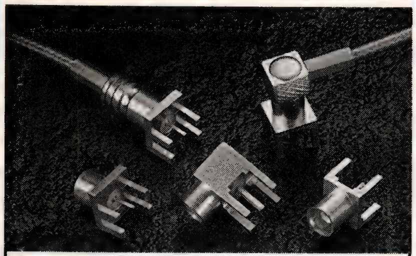

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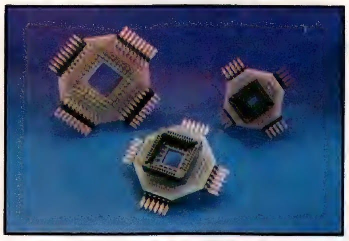

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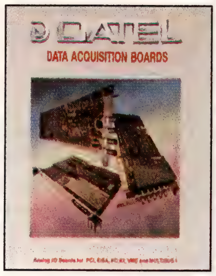

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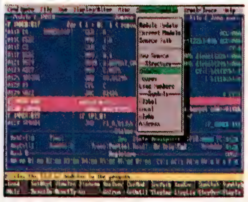

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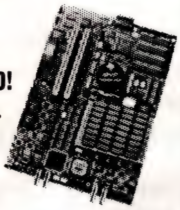

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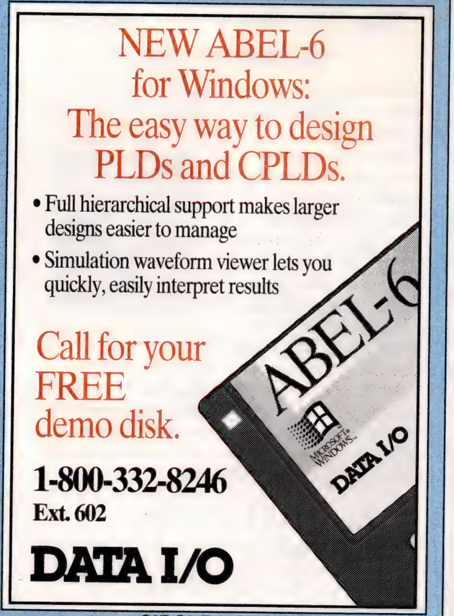
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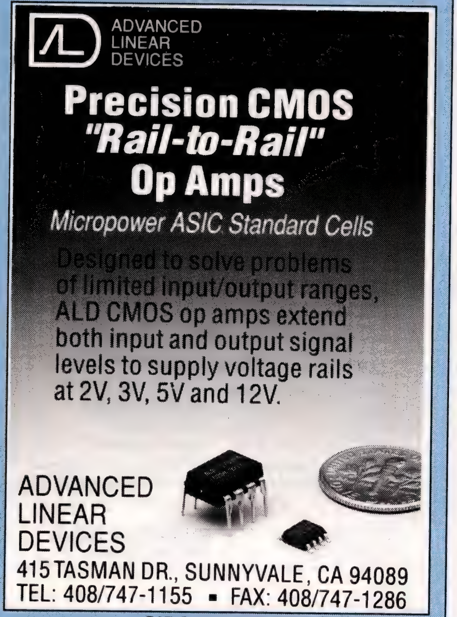
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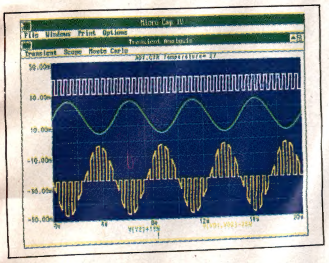

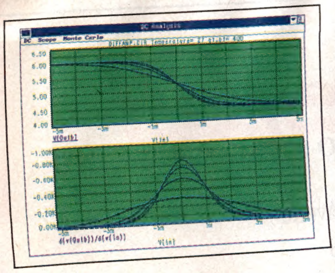

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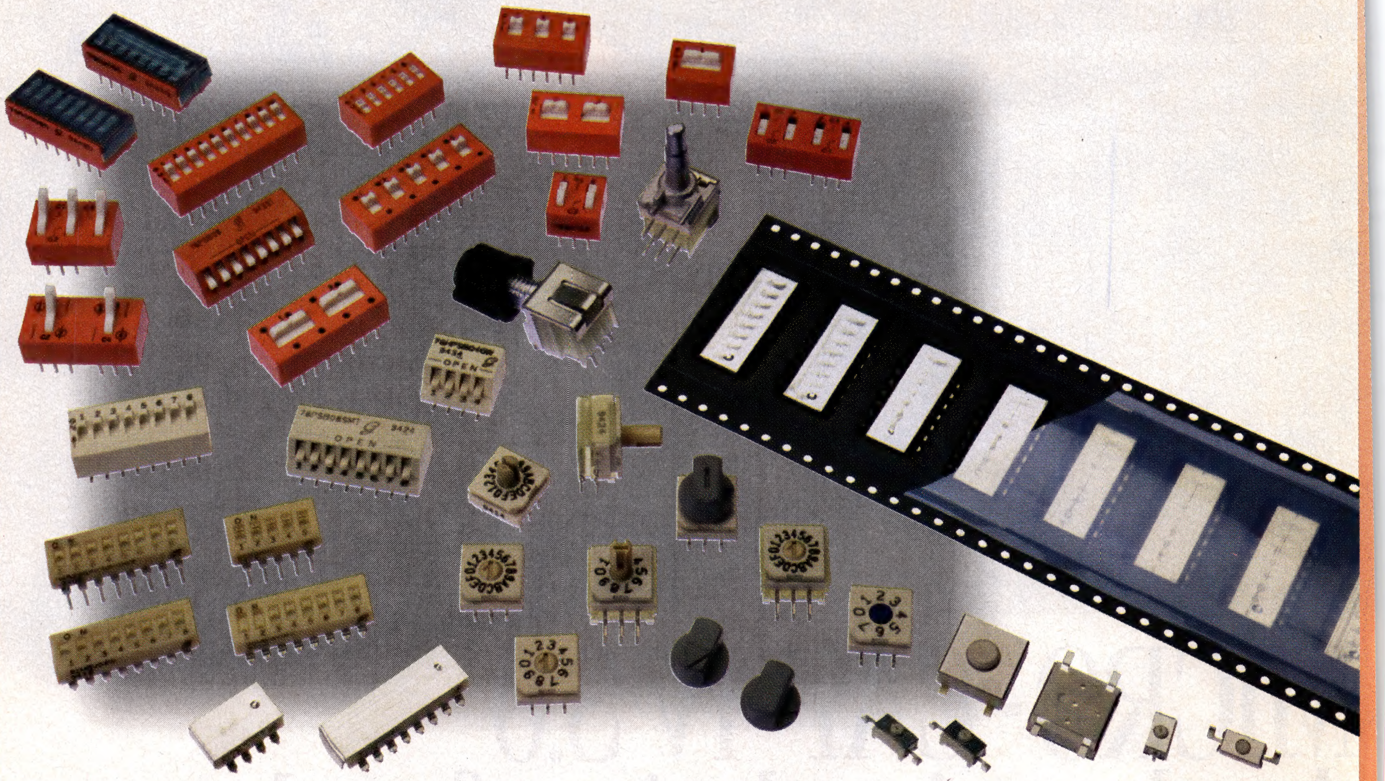

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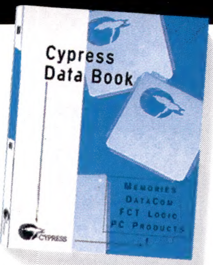

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